Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **18EI3001** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ADVANCED EMBEDDED SIGNAL PROCESSORS** | **Max. Marks :** | **100** |

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| **Q. No.** | **Sub Div.** | **Questions** | **Course Outcome** | **Marks** |
| **ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)** | | | | |
| 1. | a. | Compute 4-point DFT of causal three sample sequence.  X(n) = 1/3; 0 ≤ n ≤ 2  = 0; else | CO1 | 8 |
| b. | Design a linear phase FIR low pass filter using rectangular window by taking Z samples of window sequence and with a cutoff frequency ωc = 0.2π rad/sample. | CO1 | 8 |
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| 2. | a. | List the relative merits and demerits of RISC and CISC processors. | CO2 | 8 |
| b. | Discuss on-chip peripherals of DSP. | CO2 | 8 |
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| 3. | a. | Justify the P-DSPs have multiple address and data buses for internal memory and peripherals but have only a single address and data bus for the external memory and peripherals. | CO2 | 8 |
| b. | Draw the internal architecture of TMS320C5X processor and indicate the various blocks. | CO3 | 8 |
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| 4. | a. | What is meant by memory mapped registers? How it is different from a memory? | CO3 | 8 |
| b. | Explain the various On-chip peripherals of TMS320C5X processor. | CO3 | 8 |
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| 5. | a. | Illustrate with example the pipeline operation on ARAU memory mapped registers. | CO3 | 8 |
| b. | With functional diagram, explain MAC uit of TMS320C54X processor. | CO4 | 8 |
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| 6. | a. | With block diagram, explain the architecture of 54X processor. | CO4 | 8 |
| b. | Discuss the various data paths in TMS320C6X processor. | CO4 | 8 |
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| 7. | a. | Enumerate the pros and cons behind FPGA and programmable signal processors. | CO5 | 8 |
| b. | Discuss Xilinx 4000 FPGA structure in detail. | CO5 | 8 |
| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Discuss the importance of distributed arithmetic algorithm for embedded DSP functions in FPGA. | CO6 | 10 |
| b. | Implement serial convolver using FPGA. | CO6 | 10 |