Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **18EC3054** | **Duration :** | **3hrs** |
| **Sub. Name :** | **HIGH SPEED VLSI DESIGN** | **Max. Marks :** | **100** |

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| **Q. No.** | **Sub Div.** | **Questions** | **Course Outcome** | **Marks** |
|  |  | **ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)** |  |  |
| 1. | a. | Assess the different Non Clocked Pass Gate Families in an analog circuit and give the different types of NCGF. Also analyze the occurrence of TG Logic-DCVSPGCPL-SRPL-EEP. | CO1 | 10 |
| b. | Discuss the operation of static Complementary metal oxide Semiconductor structure DCVS. | CO1 | 06 |
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| 2. |  | Interpret the Domino approaches for the Clocked logic systle. Also briefly explain the following  i) Polarity Domino Approaches  ii) Dual-Rail Domino Structures  iii) Latched Domino Structures . | CO2 | 16 |
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| 3. | a. | Derive the circuit design margin of a high speed VLSI Design system. | CO3 | 8 |
| b. | Give an application for the design induced variation of circuit design margin. | CO3 | 8 |
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| 4. |  | With a suitable circuit diagram, explain the Latching Differential Logic circuit. Also, prove the function asynchronous Latch techniques . | CO4 | 16 |
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| 5. | a. | Discuss the problem of point to point wiring at high frequencies with necessary equations. | CO3 | 8 |
| b. | With suitable techniques, explain the interfacing techniques for receiver design technique | CO5 | 8 |
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| 6. |  | Summarize end terminations in the following respects (a) Rise time by intuition and calculation (b) DC Biasing. | CO4 | 16 |
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| 7. | a. | Explain Skin effect and its mechanics at very high speeds. | CO5 | 10 |
| b. | Explain Meta –stability in clock distribution at high speeds. | CO5 | 6 |
|  | | **COMPULSORY QUESTION (1 x 20 = 20 Marks)** |  |  |
| 8. | a. | With suitable diagrams, briefly discuss the design rules to be followed for providing stable voltage reference to the digital systems. | CO6 | 10 |
| b. | Explain the significance of timing margin at high speeds. What is Clock Jitter? | CO6 | 10 |