Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_

****

**End Semester Examination – Nov / Dec – 2019**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **18EC3049** | **Duration :** | **3hrs** |
| **Sub. Name :** | **SYSTEM ON CHIP DESIGN** | **Max. Marks :** | **100** |

**ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Describe the pipelined processor model with suitable diagram with instruction timing. | CO1 | 8 |
| b. | Explain the instruction execution process for sequential processor with necessary diagram. | CO1 | 8 |
|  |  |  |  |  |
| 2. | a. | Discuss about ideal and practical scaling used in SOCdesign. | CO2 | 8 |
| b. | Elaborate on how area, time and power parameters are traded off in processor design. | CO2 | 8 |
|  |  |  |  |  |
| 3. | a. | Explain the instruction set, interrupt and exceptions used in processor architecture. | CO3 | 10 |
| b. | Write short note on static branch prediction. | CO3 | 3 |
| c. | Justify with key reasons why soft core processors are used. | CO3 | 3 |
|  |  |  |  |  |
| 4. | a. | Describe the direct and fully associative mapping cache organization with neat sketch. | CO4 | 8 |
| b. | Explain the working of asynchronous DRAM memory module with its chip timing diagram. | CO4 | 8 |
|  |  |  |  |  |
| 5. | a. | Idenntify and explain the system level issues and specifications for selecting suitable interconnect architecture. | CO5 | 8 |
| b. | Explain the working of static and dynamic network used in NOC interconnect with necessary block diagram. | CO5 | 8 |
|  |  |  |  |  |
| 6. | a. | Narrate the various process involved in designing SOC devices using suitable flow chart. | CO6 | 10 |
| b. | Illustrate the initial design process with three processors P1, P2 and P3 using neat sketch. | CO6 | 6 |
|  |  |  |  |  |
| 7. |  | Case study the SOC design for JPEG algorithm and explain the working of JPEG based still camera using block diagram. | CO6 | 16 |
| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Describe the various functional blocks in components of system with neat sketch. | CO1 | 10 |
| b. | Write note on off-die memory system in SOC design. | CO4 | 5 |
| c. | Explain with suitable graph how chip area is related with yield. | CO2 | 5 |