Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **18EC3030** | **Duration :** | **3hrs** |
| **Sub. Name :** | **HARDWARE DESCRIPTION LANGUAGES** | **Max. Marks :** | **100** |

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| **Q. No.** | **Sub Div.** | **Questions** | **Course Outcome** | **Marks** |
| **ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)** | | | | |
| 1. | a. | List all VHDL data types and explain each data type with example. | CO1 | 10 |
| b. | Analyze the given equation and write VHDL data flow model description. | CO2 | 6 |
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| 2. | a. | Develop VHDL test bench for the following circuit.  Image result for digital combinational circuit | CO3 | 10 |
| b. | Explain the different FOR loop and WHILE loop in VHDL. Write syntax for the same. | CO1 | 6 |
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| 3. | a. | Explain the Top down methodology in Verilog HDL with example. | CO4 | 8 |
| b. | Design 4X1 Multiplexer using Verilog HDL. | CO4 | 8 |
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| 4. | a. | Write down the Verilog HDL coding for CMOS NAND, NOR gates using switch modeling. | CO4 | 8 |
| b. | Explain the Gate delays in Verilog HDL. | CO4 | 8 |
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| 5. | a. | Develop a full adder VHDL package. | CO3 | 12 |
|  | b. | Write the syntax of Selected signal assignment and Conditional signal assignment statement. | CO1 | 4 |
|  |  |  |  |  |
| 6. | a. | Design updown counter using Verilog HDL. | CO4 | 10 |
|  | b. | Explain Verilog HDL operators. | CO4 | 6 |
|  |  |  |  |  |
| 7. | a. | Analyse the following Truth table and obtain the synthesizable Behavioural VHDL code and draw the gate level representation.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | In A | In B | InC | InD | OutE | | 0 | 0 | 0 | 0 | 1 | | 0 | 0 | 0 | 1 | 1 | | 0 | 0 | 1 | 0 | 1 | | 0 | 0 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 0 | 1 | | 0 | 1 | 1 | 1 | 0 | | 1 | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 1 | 1 | | 1 | 0 | 1 | 0 | 1 | | 1 | 0 | 1 | 1 | 0 | | 1 | 1 | 0 | 0 | 1 | | 1 | 1 | 0 | 1 | 0 | | 1 | 1 | 1 | 0 | 1 | | 1 | 1 | 1 | 1 | 0 | | CO5 | 12 |
| b. | Construct entity that describes the top level for given circuit.  Use signals of data type BIT. | CO5 | 4 |
| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Explain logic Synthesis. | CO6 | 5 |
| b. | Analyze the following statements. Draw the gate level representation in RTL level.   1. module badd (sum, c\_out, a, b, cin);   output [3:0] sum;  output c\_out;  input [3:0] a,b;  input cin;  assign {c\_out,sum}=a+b+cin;  end module   1. if(s)   out=i1;  else  out=i0;  iii) always @ (Posedge clk)  q<=d; | CO6 | 15 |