Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **18EC2030** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL ELECTRONICS** | **Max. Marks :** | **100** |

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| **Q. No.** | **Questions** | **Course Outcome** | **Marks** |
| **PART – A (10X1 = 10 MARKS)** | | | |
| 1. | Convert (1010)2 binaty to decimal. | CO1 | 1 |
| 2. | List the symbols used to represent the digits in the binary number systems. | CO1 | 1 |
| 3. | Mention any two non-weighted codes. | CO2 | 1 |
| 4. | Which gate is equal to AND-invert Gate? | CO2 | 1 |
| 5. | Mention a combinational circuit that selects binary information from one of many inputs and directs it to a single output line. | CO3 | 1 |
| 6. | Draw a logic diagram of 2 x 1 lines multiplexer with its truth table. | CO3 | 1 |
| 7. | Give the excitation table for S-R flipflop. | CO4 | 1 |
| 8. | Define hold time. | CO4 | 1 |
| 9. | How many flip-flops are required to make a MOD-32 binary counter? | CO5 | 1 |
| 10. | On the third clock pulse, a 4-bit Johnson sequence is Q0 = 1, Q1 = 1, Q2 = 1, and Q3 = 0. What will be the sequence on the fourth clock pulse? | CO5 | 1 |

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| **PART – B (6 X 3 = 18 MARKS)** | | | |
| 11. | Simplify the following expression Y = (A + B) (A + C) (B + C). | CO1 | 3 |
| 12. | Convert [643]10 to Excess 3 code. | CO2 | 3 |
| 13. | Implement full adder using two half adders. | CO3 | 3 |
| 14. | Draw the logic diagram of J-K flipflop using Nand gate. | CO4 | 3 |
| 15. | Distinguish between synchronous and asynchronous counter. | CO5 | 3 |
| 16. | Classify different types of logic families. | CO6 | 3 |

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| **PART – C (6 X 12 = 72 MARKS)**  **(Answer any five Questions from Q.no 17 to 23. Q.No 24 is a Compulsory Question)** | | | | | |
| 17. | a. | Explain in detail on the various logic gates. | CO1 | 6 | |
| b. | Draw the logic diagram and truth table for the Boolean expression given:  Q=AB+AC’ | CO1 | 6 | |
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| 18. | a. | Simplify the following equation using K Map.  F(a,b,c,d) =Σ (0,1,2,8,10,11,14,15) + d(12,13) | CO2 | 6 | |
| b. | |  | | --- | | Design a 3 bit Even parity generator and checker circuit. | | CO2 | 6 | |
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| 19. | a. | |  | | --- | | Design a combinational circuit for BCD to Excess 3 code converter. | | CO3 | 6 | |
| b. | |  | | --- | | Design a data selector circuit that can select data from any one of the 4 inputs and transmit it to the single output. | | CO3 | 6 | |
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| 20. | a. | |  | | --- | | Explain the operation of S-R flipflop with logic diagram. | | CO4 | 6 | |
| b. | Realize T Flip flop using J-K flipflop. | CO4 | 6 | |
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| 21. | a. | |  | | --- | | Design a MOD 5 counter with unused states using T flipflop. | | CO5 | 6 | |
| b. | |  | | --- | | Design a 3 bit synchronous binary up-down counter using T flip flop. | | CO5 | 6 | |
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| 22. | a. | Construct full adder with truth table and logic diagram. | CO3 | 6 | |
| b. | Implement F(a,b,c,d) =Σm(1,4,5,7,9,12,13) using 4x1 multiplexer. | CO3 | 6 | |
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| 23. | a. | Explain the operation of Johnson counter. | CO5 | 6 | |
| b. | With logic diagram, discuss the operation of Serial In Parallel Out shift register. | CO5 | 6 | |
|  |  | **Compulsory:** | | | |
| 24. | a. | |  | | --- | | Implement BCD to Gray code converter using PAL. | | CO6 | | 6 |
| b. | Discuss the operation of schottky TTL.  Question No.24 from Module 6 | CO6 | | 6 |

Question No.24 from Module 6