Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **18EC2003** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL SYSTEM DESIGN** | **Max. Marks :** | **100** |

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| **Q. No.** | **Questions** | **Course Outcome** | **Marks** |
| **PART – A (10X1 = 10 MARKS)** | | | |
| 1. | What is the algebraic function of Exclusive –OR gate? | CO1 | 1 |
| 2. | List any two self-complementing codes. | CO1 | 1 |
| 3. | Define: Combinational circuit. | CO3 | 1 |
| 4. | Construct an AND gate using NAND gate. | CO1 | 1 |
| 5. | Write the excitation table of a JK Flip-Flop. | CO4 | 1 |
| 6. | Define: Trigger in a Flip-Flop. | CO4 | 1 |
| 7. | List any three logic families used in IC design. | CO5 | 1 |
| 8. | List the characteristics of the IC Logic families. | CO5 | 1 |
| 9. | Define cycle time of a memory. | CO5 | 1 |
| 10. | List the types of ROMs. | CO5 | 1 |

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| **PART – B (6 X 3 = 18 MARKS)** | | | |
| 11. | Apply DeMorgan’s theorem to find the compement of F= x + yz and prove that F.F’ = 0 | CO1 | 3 |
| 12. | Illustrate F(A,B,C) = ∑ ( 1, 3, 5, 6) with a Multiplexer. | CO3 | 3 |
| 13. | Explain the operation of a Master-Slave Flip-Flop with a block diagram. | CO4 | 3 |
| 14. | Define: Power dissipation. | CO5 | 3 |
| 15. | Distinguish between EPROM and EEPROM. | CO5 | 3 |
| 16. | Explain the port declarations for a Full adder. | CO6 | 3 |

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| **PART – C (6 X 12 = 72 MARKS)**  **(Answer any five Questions from Q.no 17 to 23. Q.No 24 is a Compulsory Question)** | | | | |
| 17. |  | Simplify the Boolean function F together with the don’t –care conditions d in   1. Sum of products and 2. Product of sums   F(A,B,C,D) = ∑ (3,4,13,15)  d(A,B,C,D) = ∑ (1, 2, 5, 6,8,10, 12, 14) | CO2 | 12 |
| 18. | a. | Design a BCD adder. | CO3 | 8 |
| b. | Design a Barrel shifter to shift a 3 –bit data to the left. | CO3 | 4 |
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| 19. | a. | Design an asynchronous MoD – 10 counter. | CO4 | 8 |
| b. | A state table is given below. Derive the reduced state table and draw the Reduced State Diagram.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Present state | Next state | | Output | | | x=0 | x=1 | x=0 | x=1 | | a | a | b | 0 | 0 | | b | c | d | 0 | 0 | | c | a | d | 0 | 0 | | d | e | f | 0 | 1 | | e | a | f | 0 | 1 | | f | g | f | 0 | 1 | | g | a | f | 0 | 1 | | CO4 | 4 |
| 20. | a. | Design a two input TTL NAND gate. | CO5 | 6 |
| b. | Compare the characteristics of TTL and CMOS Logic families. | CO5 | 6 |
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| 21. |  | A CPU operates with a clock frequency of 50 MHz. It communicates with a memory whose access time and cycle time do not exceed 50 ns. Draw the memory cycle timing waveforms. | CO5 | 12 |
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| 22. | a. | Design a synchronous sequential circuit using JK Flip-Flops, given the state diagram. | CO4 | 6 |
| b. | Design a 3-bit Johnson counter and explain its operation with a neat timing diagram. | CO4 | 6 |
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| 23. | a. | Design a 3 bit odd parity generator. | CO3 | 6 |
| b. | Design an implement a 3 bit Binary to Gray code converter on PROM. | CO5 | 6 |
|  |  | **Compulsory:** |  |  |
| 24. | a. | Develop a Verilog HDL code to design a 4 x 1 Multiplexer using Structural modeling. | CO6 | 6 |
| b. | Develop a Verilog HDL code to design a 4-bit Up Counter using Behavioural modeling.  Question No.24 from Module 6 | CO6 | 6 |