Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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|  |  |  |  |
| **Code :** | **17EC3042** | **Duration :** | **3hrs** |
| **Sub. Name :** | **SYSTEM ON CHIP DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain the static design styles of complementary gate. | CO1 | 15 |
| b. | Discuss the role of a sleep transistor in MTCMOS. | CO1 | 5 |
| **(OR)** | | | | |
| 2. | a. | Design a static complementary structure for the following logic expressions: | CO5 | 8 |
| b. | Analyze and discuss the delay through inductive interconnect with suitable diagrams. | CO1 | 12 |
|  |  |  |  |  |
| 3. |  | Explain power optimization in combinational network. | CO2 | 20 |
| **(OR)** | | | | |
| 4. |  | Discuss the testing methods in combinational network. | CO4 | 20 |
|  |  |  |  |  |
| 5. | a. | Discuss the function master and Slave flip flop and explain the same with necessary diagram. | CO2 | 12 |
| b. | Write the sequential circuit design procedure. | CO2 | 8 |
| (OR) | | | | |
| 6. |  | Describe various testing challenges and testing methodology of sequential machines. | CO4 | 20 |
|  |  |  |  |  |
| 7. |  | Sketch the structure of an 8 X 8 Wallace tree multiplier and explain its operation. | CO6 | 20 |
| **(OR)** | | | | |
| 8. | a. | Implement the following function using PLA | CO1 | 5 |
| b. | Explain Carry look ahead adder and mention its advantages. | CO1 | 15 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Explain global routing with example. | CO3 | 15 |
| b. | List out the significance of power and clock distribution in floor planning and explain any one of the distribution technique. | CO3 | 5 |