Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **17EC3030** | **Duration :** | **3hrs** |
| **Sub. Name :** | **HARDWARE DESCRIPTION LANGUAGES** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain different VHDL operators . | CO1 | 15 |
| b. | Discuss three different types of architecture modelling in VHDL. | CO1 | 5 |
| **(OR)** | | | | |
| 2. | a. | Write the syntax for the following VHDL statements and with example explain each statement.  i) If statement  ii) case statement. | CO1 | 12 |
| b. | Design decoder using VHDL. | CO2 | 8 |
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| 3. | a. | Explain usage generic in a component declaration and in a component instantiation with example. | CO3 | 10 |
| b. | Design updown counter using VHDL. | CO2 | 10 |
| **(OR)** | | | | |
| 4. |  | Design following Moore model machine using VHDL.  E:\official\LMS\moore.png | CO4 | 20 |
|  |  |  |  |  |
| 5. | a. | Explain the different Verilog HDL data types with an example. | CO1 | 15 |
| b. | Name the basic components of a module and list all the mandatory components. | CO1 | 5 |
| **(OR)** | | | | |
| 6. |  | Design 4-bit adder using Verilog HDL. | CO2 | 20 |
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| 7. | a. | Explain Various delay based timing control in Verilog HDL. | CO1 | 10 |
| b. | Design 4X1 multiplexer using Verilog HDL. | CO2 | 10 |
| **(OR)** | | | | |
| 8. | a. | Write the verilog coding for CMOS NAND, NOR gates using switch modeling. | CO5 | 14 |
| b. | Design PIPO Shift register using Verilog HDL. | CO2 | 6 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Explain Login synthesis with the help of a y chart representation and also explain High level synthesis with data flow graph. | CO6 | 10 |
| b. | For the following statements Draw the gate level representation in RTL level.  i) assign out =(a&b)│c;  ii) if(s)  out=i1;  else  out=i0;  iii) always @ (Posedgeclk)  q<=d; | CO6 | 10 |