Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **17EC2048** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | | Explain briefly the design flow process used in VHDL modeling. | CO1 | 8 |
| b. | | Design an ALU to perform the operations given in the table below.   |  |  |  |  | | --- | --- | --- | --- | | **ASEL** | **AOUT** | **LSEL** | **LOUT** | | ADD | A+B | OR1 | L OR M | | SUB | A-B | AND1 | L AND M | | MUL | A\*B | NAND1 | L NAND M | | DIV | A/B | NOR1 | L NOR M | | CO1 | 12 |
| **(OR)** | | | | | |
| 2. | | a. | Explain in detail the different scalar data types. | CO1 | 10 |
| b. | Explain briefly the various Data operators used in VHDL based system design. | CO1 | 10 |
|  | |  |  |  |  |
| 3. | | a. | Design a 4 : 1 multiplexer using behavioral modeling. | CO2 | 10 |
| b. | Write a VHDL Program for four bit full adder, using the structural description. Draw its basic structure showing the inputs and outputs signals. | CO2 | 10 |
| **(OR)** | | | | | |
| 4. | | a. | Explain in detail the Positional and Named association in Component Instantiation. | CO1 | 10 |
| b. | Explain different loop statements in VHDL with an example. | CO1 | 10 |
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| 5. | | a. | Discuss various delay models in VHDL. Write the syntax of all delay models. | CO1 | 10 |
| b. | Develop a VHDL package for halfadder circuit. | CO4 | 10 |
| **(OR)** | | | | | |
| 6. | | a. | Compare function with procedure in sub program. | CO4 | 6 |
| b. | What is test bench? Write Full adder test bench program. | CO3 | 14 |
|  | |  |  |  |  |
| 7. | | a. | Design the 4-bit shift register that will accept input data serially and gives output data serially. | CO2 | 10 |
| b. | Construct 4-bit sequential circuit using VHDL that is used to count the number of clock pulses. The up counting and the down counting process in the counter is decided by the control signal. | CO2 | 10 |
| **(OR)** | | | | | |
| 8. | | a. | Using generic statement, write the VHDL code for Multiplexer. | CO4 | 6 |
| b. | With a state transaction diagram, design a traffic light controller using VHDL. | CO2 | 14 |
|  | | | **Compulsory**: |  |  |
| 9. | |  | Discuss the Input output block and configurable logic block in detail. | CO5 | 20 |