Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2073** | **Duration :** | **3hrs** |
| **Sub. Name :** | **LOW POWER TECHNIQUES IN VLSI DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | List the approaches used in estimating the power in architectural level simulation. And also explain it with necessary power models. | CO1 | 10 |
| b. | Implement the function F=((a.(b.c)).(c.(d+e))’ using CMOS logic. | CO2 | 10 |
| **(OR)** | | | | |
| 2. | a. | Explain in detail about the transistor sizing with necessary examples. | CO2 | 10 |
| b. | Describe the power extraction methods in gate level simulation with necessary equations. | CO2 | 10 |
|  |  |  |  |  |
| 3. | a. | Predict how the precomputation can be done in synchronous digital circuit. | CO3 | 10 |
| b. | Discuss in detail about the power reduction techniques used in clock network. | CO2 | 10 |
| **(OR)** | | | | |
| 4. | a. | The gray code counters are better than the binary code counters.  Justify the statement with necessary equations, tables and explanation. | CO3 | 10 |
| b. | Explain in detail about the logic level low power design of a digital circuit. | CO2 | 10 |
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| 5. | a. | With a neat timing diagram, explain about clocking gating and glitches at pratical environment. | CO2 | 10 |
| b. | Predict how the keeper circuits are useful in CMOS floating nodes. | CO3 | 10 |
| **(OR)** | | | | |
| 6. | a. | Describe about the delay balancing approach in array multipliers. | CO2 | 10 |
| b. | Discuss in detail about the performance management scheme used in asynchronous processing unit. | CO2 | 10 |
|  |  |  |  |  |
| 7. | a. | Elaborate the issues in designing the deep submicrometer device. | CO2 | 15 |
| b. | Write a short note on leakage current in deep submicrometer. | CO2 | 5 |
| **(OR)** | | | | |
| 8. |  | Justify how the multiple threshold voltages are useful in managing the power and performance of a VLSI chip. | CO3 | 20 |
|  | | **Compulsory**: |  |  |
| 9. |  | Explain in detail about the energy recovery circuit design. | CO2 | 20 |