Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov / Dec– 2019**

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| **Code :** | **14EC2072** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALYSIS AND DESIGN OF DIGITAL IC** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Justify the statement “NMOS transistors pass strong zero but not strong one”. | CO3 | 6 |
| b. | Illustrate different regions of operation of NMOS transistor with neat diagram and necessary equations. | CO2 | 14 |
| **(OR)** | | | | |
| 2. | a. | Distinguish between linear and saturation operating modes of NMOS transistors. | CO3 | 4 |
| b. | Obtain the voltage transfer curve of CMOS inverter, analyze it and indicate the status of PMOS and NMOS transistors in different regions. | CO2 | 16 |
|  |  |  |  |  |
| 3. | a. | Mention the advantage of transmission gate logic as compared to pass transistor logic. | CO1 | 4 |
|  | b. | Illustrate the problem associated with cascading dynamic gates and provide a solution for the same. | CO2 | 16 |
| **(OR)** | | | | |
| 4. | a. | Draw the block diagram of domino logic design style. | CO1 | 4 |
|  | b. | Analyze and illustrate the different types of power dissipation that occurs in CMOS inverter design with mathematical equations. | CO2 | 16 |
|  |  |  |  |  |
| 5. | a. | Distinguish between Analytical delay model and Empirical Delay model. | CO2 | 4 |
|  | b. | Design F = ((AB)+(CD)) using domino logic design style and explain its operation. | CO1 | 16 |
| **(OR)** | | | | |
| 6. | a. | Give the relation between fall time and rise time for equally sized n and p transistors in an inverter. | CO2 | 4 |
|  | b. | Implement F=A + BCD using complementary CMOS logic design style. | CO1 | 16 |
|  |  |  |  |  |
| 7. | a. | With timing diagram explain negative latch. | CO1 | 4 |
|  | b. | Mention the need for designing a low voltage static latch. Discuss the challenges in the design and provide a solution for the same in the design. | CO3 | 16 |
| **(OR)** | | | | |
| 8. | a. | Distinguish between foreground and background memory. | CO1 | 4 |
|  | b. | Analyze the impact of clock overlap in master slave register and provide a solution for the same with neat diagram. | CO3 | 16 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Design a pipelined datapath for the computation of log(la+bl) and explain its operation by comparing it with the conventional design. | CO1 | 20 |