Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2071** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VLSI SUBSYSTEM DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Illustrate in detail the Carry Look Ahead adder. | CO2 | 10 |
| b. | Determine the design Strategies and structured Strategies in VLSI Subsystem Design. | CO1 | 10 |
| **(OR)** | | | | |
| 2. | a. | Design the binary adder and subtractor with neat diagram. | CO1 | 12 |
| b. | Design Array multiplier with neat circuit diagram. | CO2 | 8 |
|  |  |  |  |  |
| 3. | a. | Develop odd and even Parity Generators. | CO2 | 10 |
| b. | Discuss in detail the Comparators. | CO2 | 10 |
| **(OR)** | | | | |
| 4. | a. | Illustrate the Two Phase and Four Phase Clocking Schemes. | CO3 | 10 |
| b. | Develop a binary synchronous counter. | CO3 | 10 |
|  |  |  |  |  |
| 5. | a. | Explain in detail the barrel shifter. | CO3 | 10 |
| b. | Discuss in detail the Asynchronous Counter. | CO3 | 10 |
| **(OR)** | | | | |
| 6. |  | Illustrate in detail the Memory Core. | CO2 | 20 |
|  |  |  |  |  |
| 7. |  | Explain Memory Peripheral Circuit. | CO2 | 20 |
| **(OR)** | | | | |
| 8. | a. | Illustrate the different types of RAM. | CO2 | 12 |
| b. | With neat diagram, discuss ROM. | CO2 | 8 |
|  | | **Compulsory**: |  |  |
| 9. |  | Illustrate in detail the PLA Design. | CO2 | 20 |