Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2070** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ASIC DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Explain features of full custom ASIC and its types. | CO2 | 12 |
| c. | Give the important features of Gate Array Based ASIC. | CO1 | 8 |
| **(OR)** | | | | |
| 2. | a. | Explain the ASIC design flow with a neat flow diagram. | CO2 | 14 |
| b. | Give the programming step for EPROM and EEPROM. | CO1 | 6 |
|  |  |  |  |  |
| 3. | a. | Briefly explain the architecture of XC4000 Logic block ASIC’s with a neat diagram. | CO2 | 15 |
| b. | Explain the Actel Act1 architecture logic module with an illustration. | CO2 | 5 |
| **(OR)** | | | | |
| 4. | a. | Briefly describe the XILINX input output block performs of FPGA. | CO2 | 6 |
| b. | In detail give the architecture of Altera FLEX chip floorplan, LAB and logic element. | CO3 | 14 |
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| 5. | a. | Discuss the Schematic Entry for ASIC different types of objects and illustrate it with instantaneous. | CO3 | 20 |
| **(OR)** | | | | |
| 6. | a. | Give the Electronic design interchange format tools used in the ASIC design with hierarchical nature. | CO3 | 14 |
| b. | Discuss the ASIC design flow with a neat flow diagram. | CO3 | 6 |
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| 7. | a. | Explain the routing and the method to channel routing in the floor planning. | CO3 | 10 |
| b. | Describe in detail the placement algorithms and briefly explain Eigen placement algorithm. | CO2 | 10 |
| **(OR)** | | | | |
| 8. | a. | Give the iterative placement improvement algorithm in details. | CO3 | 10 |
| b. | Explain the procedure for measurement of delay in floor planning. | CO2 | 10 |
|  | | **Compulsory:** |  |  |
| 9. | a. | With an illustration, explain the special routing in an ASIC. | CO3 | 12 |
| b. | Explain in detail about any algorithm for the routing methods with a neat digram. | CO2 | 8 |