Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2069** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VLSI DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain the different fabrication steps of Silicon On Insulator (SOI) process with neat diagram. | CO1 | 12 |
| b. | Infer in detail about Gate array Layout. | CO1 | 8 |
| **(OR)** | | | | |
| 2. | a. | Explain in detail about the fabrication of p-well CMOS process with neat diagrams and construct the p-well based CMOS Inverter. | CO1 | 10 |
| b. | With neat block diagram illustrate in detail about VLSI design flow. | CO1 | 10 |
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| 3. | a. | Show the relationship between Drain-to-source current (Ids) Vs Vds in non-saturation and saturation region and find the drain current in cutoff, non saturation and saturation region. | CO1 | 12 |
| b. | Examine in detail about channel length modulation,thresholdvoltage,Drainpunchthrough and Hot electron effect of MOS transistor. | CO1 | 8 |
| **(OR)** | | | | |
| 4. | a. | With neat diagram of NMOS enhancement mode transistor,explain the regions of operation of MOS transistor for various terminal voltages. | CO1 | 12 |
| b. | Construct the small signal model for an MOS transistor and evaluate the small signal AC characteristics. | CO1 | 8 |
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| 5. | a. | Construct the circuit, stick diagram and layout of 2-input CMOS NAND Gate. | CO2 | 8 |
| b. | With neat diagram explain in detail about n-well based CMOS Layout design rules. | CO2 | 12 |
| **(OR)** | | | | |
| 6. | a. | Design CMOS logic for the following functions:  Z=(A.B) + C.(D+E)  Z=(A+B+C+D) | CO3 | 12 |
|  | b. | Develop the circuit, stick diagram and the layout of 2-input CMOS NOR Gate. | CO2 | 8 |
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| 7. | a. | Discuss in detail about CMOS Domino logic and design the following expression using the same.  Z = *AB + (C + D)(E + F) + GH* | CO2 | 14 |
| b. | Design 3-input NAND gate using Dynamic CMOS logic | CO2 | 6 |
| **(OR)** | | | | |
| 8. | a. | With neat diagram summarize aboutclocked CMOS logic (C2MOS) and design 3-input NAND gate using clocked CMOS (C2MOS) logic. | CO2 | 12 |
| b. | With neat timing diagram , demonstrate about np-CMOS logic. | CO2 | 8 |
|  | | **Compulsory**: |  |  |
| 9. | a. | With advantages and disadvantages explain in detail about pseudo NMOS logic. | CO2 | 8 |
| b. | Illustrate in detail about Dynamic CMOS logic and design the following Boolean expression using Dynamic CMOS Logic.  F = (A1.A2.A3) + (B1.B2) | CO2 | 12 |