Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | List the various operators and its operation in VHDL. | CO1 | 10 |
| b. | Construct a half adder circuit using VHDL structural modeling. | CO2 | 10 |
| **(OR)** | | | | |
| 2. | a. | List the various Data types in VHDL. | CO1 | 10 |
| b. | Design a 4X1 Multiplexer circuit using VHDL structural modeling. | CO2 | 10 |
|  |  |  |  |  |
| 3. | a. | Design the following combinational circuit using VHDL Data flow modeling. Each gate has a 5 ns delay and the inverter has a 2 ns delay. | CO3 | 10 |
| b. | Discuss various delay models in VHDL. Write the syntax of all delay models. | CO1 | 10 |
| **(OR)** | | | | |
| 4. | a. | Give syntax for the following VHDL statements and with example explain each statement:  i) If statement. ii) Case statement. | CO1 | 16 |
| b. | Distinguish thefollowing in terms of simulation:  i) Dataflow and behavioral model.  ii) Variable and signal Assignment statement. | CO1 | 4 |
|  |  |  |  |  |
| 5. | a. | Develop 8X3 encoder using VHDL. | CO2 | 10 |
| b. | With one example explain all the loop statements in VHDL. | CO1 | 10 |
| **(OR)** | | | | |
| 6. | a. | Develop full adder test bench. | CO1 | 10 |
| b. | Develop JK-Flipflop using VHDL | CO1 | 10 |
|  |  |  |  |  |
| 7. | a. | Design the 4-bit shift register that will accept input data serially and gives output data serially. | CO2 | 10 |
| b. | Construct 4-bit updown counter using VHDL that is used to count the number of clock pulses. The up counting and the down counting process in the counter is decided by the control signal. | CO2 | 10 |
| **(OR)** | | | | |
| 8. | a. | Design the 4-bit shift register that will accept input data serially and gives output datain parallel. | CO2 | 10 |
| b. | Develop 3X8 Decoder using VHDL. | CO2 | 10 |
|  | | **Compulsory**: |  |  |
| 9. |  | Design Traffic light controller circuit using VHDL. | CO3 | 20 |