Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2067** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VERILOG HDL** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Demonstrate in detail about the design of full adder and write the gate-level modeling using Verilog. | CO2 | 8 |
| b. | Demonstrate in detail about the design of 4-bit ripple carry adder and write the gate-level modeling using Verilog. | CO2 | 8 |
| c. | Illustrate about the different types of Gate delays. | CO1 | 4 |
| **(OR)** | | | | |
| 2. | a. | Outline in detail about the Integer, Real and Time Register Data types and Arrays in Verilog with suitable examples. | CO2 | 8 |
| b. | Construct full subtractor and write the gate-level modeling using Verilog. | CO2 | 8 |
| c. | Write the module definition for the module shift\_reg. Include the list of ports and port declarations. | CO2 | 4 |
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| 3. | a. | With neat examples examine relational, bit-wise operators , shift operators and equality operators. | CO2 | 6 |
| b. | Design a 2-bit magnitude comparator using CASE statements. | CO2 | 6 |
| c. | Develop a Verilog code in behavioral modeling for BCD to seven segment display. | CO2 | 8 |
| **(OR)** | | | | |
| 4. | a. | Design a 4-bit ripple counter using negative edge triggered D flip-flop and construct the design in Verilog. | CO3 | 10 |
| b. | Develop a Verilog code for a counter which increments the count from 0 to 127 and exit at count 128 using forever loop. | CO3 | 4 |
| c. | Construct 4x1 mux using Conditional Operators only. | CO2 | 6 |
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| 5. | a. | Write the Verilog program in behavioral modeling for T-Flip-flop with positive edge triggered clock. | CO2 | 4 |
| b. | Develop a Switch-Level Verilog Description of 2-to-l Multiplexer. | CO2 | 8 |
| c. | Summarize in detail about Bidirectional Switches ,Power and Ground used in switch level modeling. | CO2 | 8 |
| **(OR)** | | | | |
| 6. | a. | Describe about the Conditional Statements in verilog with neat examples. | CO2 | 8 |
| b. | Develop a 8-bit ALU for reset, preset, addition, subtraction, AND,XOR,OR and XNOR operation. | CO2 | 10 |
| c. | Illustrate in detail about CMOS Switches. | CO2 | 2 |
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| 7. | a. | Examine about always and initial statement in behavioral modeling. | CO2 | 10 |
| b. | Design Z=(A.B)+(C.D) E using CMOS Logic and write switch level Verilog Description. | CO3 | 10 |
| **(OR)** | | | | |
| 8. |  | Design Finite State Machine for Newspaper Vending Machine and write the Verilog Description. | CO3 | 20 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Illustrate about test bench and develop the test bench for 4-bitripple carryadder. | CO3 | 10 |
| b. | Develop a Switch-Level Verilog description of CMOS Flip-flop. | CO3 | 10 |