Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14EC2066** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL SYSTEM DESIGN** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Distinguish between combinational and sequential logic circuits. | CO1 | 4 |
| b. | Design a Full subtractor circuit. | CO1 | 16 |
| **(OR)** | | | | |
| 2. | a. | Sketch the block diagram of a sequential logic circuit. | CO1 | 4 |
| b. | Design a 3 bit up counter using T flip flop. | CO1 | 16 |
|  |  |  |  |  |
| 3. | a. | Distinguish between Mealy and Moore machine. | CO1 | 4 |
| b. | With neat timing diagram, design a BCD ripple counter. | CO1 | 16 |
| **(OR)** | | | | |
| 4. | a. | List the advantages of state table minimization. | CO1 | 4 |
| b. | With neat timing diagram, design a 4 bit ripple counter. | CO1 | 16 |
|  |  |  |  |  |
| 5. | a. | Distinguish between synchronous and asynchronous sequential logic circuits. | CO1 | 4 |
| b. | Implement the function F(A,B,C) = A+BC on a PROM architecture. | CO3 | 16 |
| **(OR)** | | | | |
| 6. | a. | Distinguish between fundamental mode and pulse mode asynchronous sequential logic circuits. | CO1 | 4 |
| b. | Implement a one bit full adder circuit on a PAL architecture. | CO3 | 16 |
|  |  |  |  |  |
| 7. | a. | List different types of PLDs and expand the same. | CO2 | 4 |
| b. | Implement the functions F1(A,B,C) = ∑ (0,1,5,6) and F2(A,B,C) = π (0,1,5,6) on a PLA architecture. | CO3 | 16 |
| **(OR)** | | | | |
| 8. | a. | Distinguish the types of PLDs with respect to its architecture. | CO2 | 4 |
| b. | Design an ASM chart for the state diagram in Fig.1.    Fig. 1 | CO3 | 16 |
|  | | **Compulsory:** |  |  |
| 9. |  | With neat diagram, illustrate the operation of Altera MAX CPLD architecture. | CO3 | 20 |