Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **17CS2003** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain the role of PC,IR,MAR,MBR,IOAR and IOBR registers in execution of instructions with an example. | CO1 | 10 |
| b. | Discuss the sequential and nested handling of interrupts when multiple interrupts in pending with suitable diagrams. | CO4 | 10 |
| **(OR)** | | | | |
| 2. | a. | Following are the main memory locations of RAM identified by the addresses.    Complete the steps regarding addition operation.  Explain the steps with diagram for above mentioned values. | CO3 | 10 |
| b. | Elaborate how the cache memory determines the presence of a main memory block in the cache memory line using direct mapping and associative mapping techniques. | CO6 | 10 |
|  |  |  |  |  |
| 3. | a. | Justify the mandate of IO modules in the computers. Discuss the architecture of a peripheral and IO modules with a block diagram. | CO1 | 10 |
| b. | Differentiate SRAM and DRAM with suitable diagrams. | CO1 | 5 |
| c. | Describe the DMA controller with a neat sketch. | CO1 | 5 |
| **(OR)** | | | | |
| 4. | a. | Discuss the programmed and interrupt driven IO mechanisms with suitable diagrams. | CO2 | 10 |
| b. | Consider a data word 10010011 to be stored into RAM. Compute the hamming code to be stored and after the retrieval.    Calculate the syndrome word and determine the position of the error if the data word is read as 11010011. | CO1 | 10 |
|  |  |  |  |  |
| 5. | a. | Explain Booth’s multiplication algorithm with the expression 4×-3. | CO3 | 12 |
| b. | Evaluate the following expression using instructions following two address and three address instruction formats. | CO3 | 8 |
| **(OR)** | | | | |
| 6. | a. | Draw and explain the flowchart of restoring unsigned division algorithm using 7/3. | CO3 | 12 |
| b. | List and explain any three addressing modes using registers as the location of the operands with necessary diagrams. | CO3 | 8 |
|  |  |  |  |  |
| 7. | a. | Discuss the role of various user visible, control and status registers in instruction execution. | CO1 | 10 |
| b. | Design and explain the operating principle of a six stage instruction pipeline with suitable diagrams. | CO2 | 10 |
| **(OR)** | | | | |
| 8. | a. | Define hazards in pipeline. Explain the various pipeline hazards with examples and propose the solutions to overcome the hazards. | CO2 | 12 |
| b. | Discuss the indirect and interrupt cycles with suitable diagrams. | CO4 | 8 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Explain the microoperations involved in fetch and indirect cycles with pseudocode samples. | CO5 | 10 |
| b. | Differentiate the hardwired and microprogrammed control unit configurations with necessary diagrams. | CO5 | 10 |