Reg. No. \_\_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov / Dec – 2019**

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| **Code :** | **14CS2005** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. Marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | The following diagram shows the initial positions of memory and CPU registers. An addition program is stored in memory locations 100, 101 and 102. The values are stored in memory locations 540 and 541.  Explain the steps during program execution and show the final values in all these memory locations after program execution.  Given the opcode values 0001- load AC from memory,  0010- store AC to memory, 0101- add AC to memory.  100-1540  101-5541  102-2541  .  .  540-0006  541-0003 | CO1 | 15 |
|  | b. | Briefly describe the main structure and functions of computer components with a neat sketch. | CO1 | 5 |
| **(OR)** | | | | |
| 2. | a. | Consider the following:  Main memory size : 16 MB  Cache memory size : 16 KB  Block size : 4Bytes  Mapping Function : Direct Mapping   1. Calculate the address bits required for main memory 2. Calculate the number of cache lines in cache memory   Calculate the tag bit size. | CO3 | 15 |
| b. | Explain the various stages of instruction cycle with suitable diagram. | CO1 | 5 |
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| 3. |  | Consider the following for bit positions for 8 bit data:  8 Bit Data: 1010 1111 for the storage.  Calculate the check bit for the above data bits.  The following is found while reading the same data bits from the storage:  0010 1111  Calculate the check bit for the data that is read from storage.  Calculate the syndrome word from the above 2 check bits and find  where the error is? Explain with step by step procedure. | CO3 | 20 |
| **(OR)** | | | | |
| 4. | a. | Discuss with suitable diagrams, the DMA mechanism in bye-passing the involvement of processor in any input or output operation. | CO2 | 10 |
| b. | Discuss the major functions of I/O module with its general block diagram. | CO2 | 10 |
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| 5. |  | Explain the Booth’s algorithm with suitable flowchart and also compute the product of -7 and -3. | CO3 | 20 |
| **(OR)** | | | | |
| 6. | a. | Explain the following Addressing modes and illustrate the diagram for each addressing mode.  i) EA = (R) ii) EA = (A) iii) EA = A. | CO3 | 15 |
| b. | Explain the logical right shift and arithmetic shift for the following  01111011. | CO2 | 5 |
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| 7. | a. | Compare the performance of a processor with and without instruction pipelining with the suitable diagram. | CO2 | 15 |
| b. | Write short notes on user visible registers. | CO2 | 5 |
| **(OR)** | | | | |
| 8. | a. | Discuss the different pipeline hazards with necessary examples and explain the methods of resolving the data hazards. | CO3 | 15 |
| b. | Explain the branch penalty in instruction pipeline with suitable examples. | CO3 | 5 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Analyze the difference between hardwired implementation and a micro programmed implementation of a control unit with a neat diagram. | CO3 | 15 |
| b. | List the advantages and disadvantages of using a variable-length instruction format. | CO3 | 5 |