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End Semester Examinations - Nov-Dec 2015 Exams

14EC1001 Basic Electronics Engineering

Set A **Time : 3 hrs**
Total Marks: 100

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1. a) Discuss the formation of P type and N type semiconductors with neat diagram. (10)

   b) Compare the constructional features and charactestististcs of

   i)Ceramic Capacitors ii)Plastic Capacitors (10)

OR

2. a) Explain in detail the various types of resistors with necessary diagram. (14)

   b) Elucidate the various types of inductors in detail. (6)

3. a) Explain the operation and characteristics of Junction Field Effect Transistor. (14)

   b) Describe about the Half Wave Rectifier in detail with neat waveforms .(6)

OR

4. a) Explain the characteristics of Uni Junction Transistor with neat diagram. (8)

   b) With the neat circuit diagram explain the input and output characteristics of NPN transistor in CB configuration. (12)

5. a) Simplify using K-map:

   $F(a, b, c, d)=\sum(0,1,2,3,4,5,6,7)$. (10)

   b) Design a 4x1 Multiplexer and explain its operation with neat Logic diagram. (10)

OR

6. a) Simply the following using Boolean algebra

   (i)$A+AB+AB^{I}C$ (ii) $AB+A^{I}C+BC$ (10)

   b) Design a 1x4 Demultiplexer and explain its operation with neat logic diagram .(10)

7. a) Derive the expression of Amplitude modulation and its power calculation with neat waveforms. (14)

   b)What is the need for modulation? (6)

OR

8. a) Draw the block diagram and explain about the Amplitude Modulation Transmitter .(6)

   b) Derive the expression of Frequency modulation with necessary waveforms. (14)

9. a) Briefly discuss about Television Tranmitter and Receiver with neat diagram. (14)

   b) Draw and explain the block diagram of a Radar System. (6)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2001 Digital Electronics

Set A

Time : 3 hrs
Total Marks: 100

1. a. Find the canonical product of sum (POS) form and sum of product (SOP) form of the function $F(A,B,C) = (\overline{A}).(B+\overline{C})$ (7+8)

   b. Minimize the Boolean function $F = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$ using k-map. (5)

OR

2. (i). Prove the following Boolean identities. (8)

   $(x_1 + x_2)(\overline{x_1}\,\overline{x_3} + x_3)(\overline{x_2 + x_1 x_3}) = \overline{x_1}\,x_2$

   (ii). Perform the following conversion (3+3+3+3)

   a. 2F3 hex to decimal
   b. 2D5 hex to binary
   c. 235 decimal to hexadecimal
   d. 237 octal to decimal.

3. a. Simplify the Boolean function using suitable Karnaugh Map

   F(A,B,C,D,E)=Σm(3,5,6,8,9,12,13,14,19,22,24,25,30) (12)

   b. Draw the Truth Table for full adder and obtain the expressions for SUM and carry and draw the gate realization for it. (8)

OR

4. a. Simplify the following Boolean functions using Quine-McCluskey method.

   F(w,x,y,z) = Σ (0, 1, 2, 8, 10, 11, 14, 15) (10)

   b. Design a binary to gray code converter for 3 bits and implement the same using gates. (10)

5. a. Design a 2 bit Magnitude Comparator Circuit. (16)

   b. Draw the block diagram of 4bit binary parallel adder circuit. (4)

OR

6. a. Design a 1 to 4 Demultiplexer circuit. (10)

   b. Realize the function Σ(0,1,3,5,11,15) using multiplexer

7. a. Construct the state diagram for the system described in the state table given below. Note that x is the input and A and B are the state variables. (6)

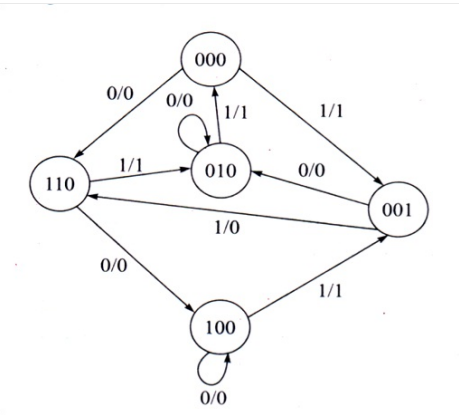
Present values			Next state	
x(t)	A(t)	B(t)	A (t+1)	B (t+1)
0	0	1	0	0
0	0	0	1	1
0	1	1	1	0

0	1	0	0	1
1	0	1	1	1
1	0	0	1	0
1	1	0	0	1
1	1	1	0	0

b. With neat diagram, explain the operation of synchronous BCD counter in detail. (14)

OR

8. a. Design a sequential logic circuit using J-K flip-flops for the state diagram shown: (12)



b. Implement a modulus 12 asynchronous counter using T flip flop. (8)

9. a. A combinational circuit is defined by the functions: F_1 (A, B, C) = Σ (3, 5, 7)

F_2 (A, B, C) = Σ (4,5, 7). Implement the circuit with a PLA having three inputs, three product terms and two outputs. (10)

b. Design and explain the operation of a CMOS NAND & NOR gates. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2002 Electron Devices

Set B

Time : 3 hrs
Total Marks: 100

1. A. Derive the thermal equilibrium concentration of holes (p_0) with the band structure showing the distribution of electrons and holes. (14)
   B. Determine the n_0p_0 product for intrinsic semiconductor.(6)

OR

2. A. With the energy band structure derive the mathematical equation for electron concentration in a compensated semiconductor (14)
   B. Calculate the thermal equillibrium electron and hole concentration in a compensated semiconductor. Consider silicon at T=300k in which $N_a = 10^{16}$ cm^{-3} and $N_d = 3 \times 10^{15}$ cm^{-3}. Assume $n_i = 1.5 \times 10^{10}$ cm^{-3}. (6)

3. A. Derive the continuity equation for holes in the body of a semiconductor as a function of time and distance. (12)
   B. Explain in detail about methods of recombination of electrons and holes with neat diagrams.(8)

OR

4. A. Explain the principle of Hall Effect and derive the expression of Hall voltage and Hall Coefficient .Also mention the significance of the Hall Effect. (14)
   B. Describe about quasi-fermi energy level with related expressions. (6)

5. A. Explain the working principle of PN diode under forward and reverse biased conditions with its volt-ampere characteristics.(14)

   B. Consider a germanium p-n junction at 300^0K with doping concentration $N_A=1.5\times10^{18}cm^{-3}$ and $N_D=2\times10^{15}cm^{-3}$ in the p and n sides of the junction respectively. Determine the contact potential (V_0) across the junction. Assume the intrinsic carrier concentration of germanium $n_i=2.5\times10^{13}cm^{-3}$ at 300^0K. (6)

OR

6. A. With neat diagrams, explain the operation , input and output characteristics of NPN transistor in CE configuration. (15)
   B. Compare CB, CE and CC transistor configurations. (5)

7. A. Explain the operation of JFET with necessary circuit diagram. Also mention the applications of the same. (15)
   B. Differentiate enhancement and depletion MOSFET. (5)

OR

8. A. Explain the current components of PNP transistor with neat diagram and define the various parameters which relate the current components. (14)
   B. Draw the Eber's moll model for NPN transistor and PNP transistor. (6)

9. A. Explain the construction and operation of Uni junction transistor with necessary circuit diagram. Also list out the applications. (12)
   B. Explain the construction and operation of LED. Also mention its advantages. (8)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2003 Signals and Systems

Set A **Time : 3 hrs**
Total Marks: 100

1. (a) Explain the following basic operations on the signal with examples.

i. Addition ii. Multiplication iii. Time shifting iv. Time scaling v. Time reversal (10)

(b) Write the mathematical definition and diagram for the following elementary signals in continuous and discrete form

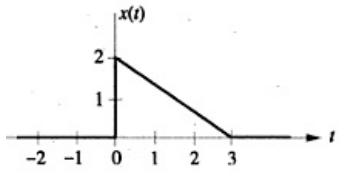
i. Unit step ii. Unit ramp iii. Unit impulse iv. Sinusoidal signals v. Exponential signals (10)

OR

2. (a) Find whether the given y(t) is (a) Time-invariant (b) static (c) Linear (d) causal (e) stable and justify.

$y(t) = x(t+10) + x^2(t)$ (10)

(b) Find (a) x(-2t-1) (b) x(2(t-1)) (c) x(t) u(t-2) from the following figure. (10)



3. (a) Determine the Fourier transform of the continuous time signal $x(t) = e^{-2|t|}$

Plot the magnitude and phase spectrum. (8)

(b) State and prove differentiation in time property of Fourier transform. (6)

(c) Find the Fourier Transform of the function $f(t) = e^{-at}\cos(bt)\,u(t)$ (6)

OR

4. (a) Determine the output response of the system whose impulse response,

$h(t) = e^{-at}\,u(t)$, $a>0$

$x(t) = e^{-bt}\,u(t)$, $b>0$ (12)

(b) Find Fourier transform and plot the magnitude spectrum for the given signal. (8)

$$x(t) = \begin{cases} 1 & -1 \le t \le 1 \\ 0 & elsewhere \end{cases}$$

5. (a) Explain the properties of ROC in Z-transform. (5)

(b) Find the Z-transform and ROC for the signal $x(n) = (-a)^n u(-n-1)$ (5)

(c) Find the inverse Z-transform of

$$X(z)=\frac{\frac{1}{4}z^{-1}}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{4}z^{-1}\right)}$$ (10)

OR

6. (a) Find the Z-transform of the signal x(n) = sin(bn) u(n). (5)

(b) What is the relationship between DTFT and Z-transform? (3)

(c) Using long division, determine the inverse Z-transform of if (i) x(n) is causal (ii)x(n) is anticausal

$$X(z)=\frac{1+2z^{-1}}{1-2z^{-1}+z^{-2}}$$ (12)

7. (a) Find the Laplace transform for the following continuous time signals (10)

(i) $x(t) = e^{-5t}[u(t) - u(t-5)]$

(ii) $x(t) = 10u(t) - 10\,e^{-t}u(t)$

(iii) $x(t) = e^{-3t}u(-t) - e^{-2t}u(-t)$

(b) State and prove any three properties of Laplace transform. (10)

OR

8. (a) Find the inverse Laplace transform:

$$X(s)=\frac{s+2}{(s^3+7s^2+15s+9)}$$ (10)

(b) Describe the different sampling methods. With neat diagrams, explain impulse train sampling. (10)

9. (a) i. Find the DTFT of (6)

$$x(n)=sin\left((\pi n/2)\right)u(n)$$

ii. Define discrete-time Fourier transform pair. (2)

(b) Determine the DTFT of the following signal,

i. x(n) = u(n-3) – u(n-5)

ii. $$x(n)=\begin{cases} n, -3 \le n \le 3 \\ o, otherwise \end{cases}$$ (12)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2006 Electronic Circuits

Set B

Time : 3 hrs
Total Marks: 100

1. Explain the working principle of Half wave rectifier and derive its rectifier efficiency, ripple factor, and transformer utilization factor .Also discuss the merits and demerits of the circuit. (20)

OR

2. A. With neat diagram explain the operation of controlled transistor series regulator and derive the output voltage expression. (12)

   B. A full wave rectifier with a load resistance of 15 Kohm uses an inductor filter of 15 H. The peak value of the applied voltage is 250 V and the frequency is 50 cycles/second. Calculate the dc load and ripple factor. (8)

3. A. Explain the voltage divider biasing for FET and show the mathematical approach for calculating the drain current. (15)
   B. What are limitations of fixed biasing in FET? (5)

OR

4. A. With neat diagram explain the operation of Full wave rectifier. Also discuss the limitations, advantages and applications of the circuit. (15)
   B. How capacitor is used in full wave rectifier to remove the ripples? (5)

5. A. Calculate $\mathbf{I_B}$ for voltage divider biasing of BJT with the following specifications. (14)

   V_{cc} = 22 V, R_1 = 39 KΩ, R_2 = 3.9 KΩ, R_c = 10 KΩ, R_E = 1.5 KΩ, β = 140

   B. Discuss the variation of Q point with respect to V_{cc} , I_B and R_c of the circuit. (6)

OR

6. Mention the special features of a power transistor and derive the collector efficiency of series fed and transformer coupled class-A power amplifier. (20)

7. What are the advantages of negative feedback in a system? Derive the gain, input impedance and output impedance for voltage shunt and series feedback connection. (20)

OR

8. Explain the operation of Differential amplifier and derive the AC voltage gain for all the three modes of operation. (20)

9. A) The tuned collector oscillator circuit used in the local oscillator of radio receiver makes use of an LC tuned circuit with L=58.6 μH and C=300 pF. Calculate the frequency of oscillation. (6)

   B) With neat sketch explain the single tuned transistor amplifier. Mention the requirements and applications of the circuit. (14)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2007 Transmission Lines and Wave guides

Set B

Time : 3 hrs
Total Marks: 100

1. A generator of 1.0V,1000 cycles, and supplies power to a 100 mile open wire line terminated in 200Ω resistance.The line parameters are: R = 10.4 Ω/mile, L = 0.00367 H/mile,G = 0.8×10^{-6} mho/mile, C = 0.00835 μf/mile

   Calculate

   a. Characteristic Impedance Z_0 (2 marks)

   b. Propagation Constant γ (2 Marks)

   c. Magnitude of Reflection co-efficient (2 Marks)

   d. Sending end current (2 Marks)

   e. Receiving end current (3 Marks)

   f. Input Power (3 Marks)

   g. Delivered power (3 Marks)

   h. Power Efficiency (3 Marks)

OR

2. Derive Campbell's equation for an equivalent T section of a transmission line consisting partially of lumped and partially of distributed elements. (20 Marks)

3. A 50 Ω lossless line is terminated in a load impedance of 25+j50 Ω. Use the smith chart to find the following, given the length of the line is 3.3λ long

   i) Locate the load impedance and admittance (4 Marks)

   ii) VSWR circle (2 Marks)

   iii) Vmax and Vmin (2 Marks)

   iv) Normalized input impedance and input admittance (2 Marks)

   v) Input Impedance and admittance (4 Marks)

   vi) Magnitude and angle of Voltage reflection coefficient at source and load (4 Marks)

   vii) Draw the length of the line from source to load along the wavelength scale. (2 Marks)

OR

4. i) Discuss in detail how impedance is matched in a transmission line using single stub matching. Derive the expressions for

   a) Length of the stub (8 Marks)

   b) Position of the stub (8 Marks)

   ii) Define skin effect and skin depth (4 Marks)

5. (i) For a frequency of 6000 MHz and plane separation of 7cm, find the following for TE_{10} mode,

Calculate the following : [10 marks]

[a] Cutoff frequency

[b] Phase velocity

[c] Is it possible to propagate TE_{31} mode?

(ii) Let us assume that, between parallel conducting plates, the E field and H field are perpendicular to each other and both of them are perpendicular to the direction of propagation also. Which type of electromagnetic wave is this? Find the following for this electromagnetic wave if air is the dielectric medium between the parallel conducting plates. [10 marks]

[a] Propagation constant, γ

[b] Phase constant, β

[c] Velocity of propagation, v

[d] Cutoff frequency,f_c

OR

6. Let us consider a parallel plane conducting guiding medium where there is electric field component in the direction of propagation but no magnetic field component in the propagation direction. Start with Maxwell's equations and develop a wave equation. Make the choice of coordinates in such a way that boundary conditions can be easily applied later. Introduce the restrictions of harmonic variations with respect to time and a wave travelling in Z direction. Determine the field equations in this case. Also sketch the field excitation for the dominant mode. [20 marks]

7. What are TM waves? Derive the electric and magnetic field equations of a Transverse Magnetic wave in a rectangular waveguide. Also discuss about its dominant mode. (20 Marks)

OR

8. An X-band waveguide which is air filled has inner dimensions of a=2.286 cm and b = 1.016 cm. Calculate the cut-off frequencies of the following modes: TE_{10}, TE_{20}, TE_{11}, TM_{11}, TM_{21} and TM_{12}. Also find out which of the modes will propagate along the waveguide and which of them will evanesce, when the signal frequency is 10GHz? If the waveguide is filled with a non-magnetic material with $\varepsilon_r = 4$, determine the effect on the cut-off frequencies for the propagating modes.
(20 Marks)

9. Briefly discuss about the following microwave lines:

a) Cavity Resonators(5 Marks)
b) Strip Lines(5 Marks)
c) Microstrip Lines (5 Marks)
d) Fin Lines (5 Marks)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2008 Linear Integrated Circuits

Set B **Time : 3 hrs**
Total Marks: 100

1. a. Explain the following electrical parameters related to ideal op-amp: (20)

   a. Input bias current b. Input offset current c. Input offset voltage d. Thermal drift

OR

2. a. Explain the working of precision half wave rectifier with necessary circuits and waveforms. (10)

   b. How can the multiplier IC be configured as a divider? Draw the diagram and derive the expression for the divider circuit. (10)

3. a. Draw and explain the operation of triangular wave generator and obtain an expression for frequency of oscillation. (10)

   b. (i) Write short note on regenerative comparator. (5)

   (ii) State the Barkhausen criteria for oscillation and construct a wien bridge oscillator for f_0 = 500 Hz. (5)

OR

4. a. Explain in detail the working of an RC phase shift oscillator with a neat circuit. Derive the frequency of oscillation. (20)

5. a. With a neat circuit, explain the operation of a second order active HPF and derive its transfer function.(10)

   b. (i) Design a second order Butterworth Low Pass Filter having upper cut off frequency

   2.5 kHz. (5)

   (ii) Write short notes on band pass filters. (5)

OR

6. a. Design a wide band pass filter having f_l = 400Hz, f_h = 2 kHz and pass band gain of 4. Find the value of Q. (10)

   b. (i) Derive an expression for the transfer function of a first order low pass filter. (5)

   (iii) List the merits of active filters over passive filters?. Classify active filters based on the range of frequency passed and draw its ideal characteristics. (5)

7. Sketch the functional diagram of a 555 timer and explain how it works as an astable multivibrator. Derive the expression for the Time period. (20)

OR

8. a. Explain the operation of IC555 timer in its monostable mode and find pulse width $t_{p.}$ (10)

   b. With relevant block diagram, explain the functionality of a PLL. (10)

9. Draw the schematic of a DAC and explain any two resistive techniques to implement DAC (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2009 Microprocessor and Interfacing techniques

Set B

Time : 3 hrs
Total Marks: 100

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1. a) Draw the architecture of 8085 and briefly explain the functional blocks.(10)

b) (i) An 8085 assembly language program is given below. Assume that the carry flag is initially unset. The content of the accumulator after the execution of the program is(4)

```
MVI A,07H
RLC
MOV B,A
RLC
RLC
ADD B
RRC
```

(ii) Calculate the number of T-states for the following instructions (6)

1. MVI A, 00 H
2. LDA 4300 H

OR

2. a)(i) Write an ALP to perform 2's complement of any number, both in 8085 and 8086. (5)

(ii) Write an assembly level program to add "N" numbers stored consecutive memory location.(5)

b) Explain the addressing modes of 8085 with two examples each. (10)

3. a)Mention the addressing modes for the following instructions(10)

1. HLT
2. XCHG AX,[BX]
3. XCHG AL,BL
4. REP STOSB
5. JMP[0AH]
6. MOV DX,[1700]
7. MOV AX,4[BX]
8. IN AX,[BX]
9. MOV AX,1234
10. MOV AL,05

b)(i) Explain about the registers available in 8086. (6)

(ii) Calculate 20-bit physical address, given that CS = 4000 H, IP = 1234 H. (4)

OR

4. . a) With a neat diagram, Explain the architecture of 8086 microprocessor.(10)

b) What is meant by addressing mode? Explain the various addressing modes in 8086 with an example. (10)

5. a) Draw a neat sketch of 8255 and explain its various modes of operation. (10)

b) (i) Write the control word to set PC_7 and reset PC_3.(4)

(ii) A 4x4 keypad is connected to port A and led is connected to port B of 8255, write the control word for the operation of mode 0 in I/O. (6)

OR

6. a) Draw and explain the block diagram of 8251-USART (10)

b) (i)Give the function of any 5 signals which is associated with serial data transfer using 8251. (5)

(ii) Find the control word for 8251A command instruction when internal reset and error reset are set to high.(5)

7. a) Draw and explain the block diagram of 8253-programmable interval timer. (10)

b) Write the control word for the following cases: (10)

i) Counter 0 in mode 1 with count value 05H

ii) Counter 1 in mode 2 with count value 65536H

iii) Counter 2 in mode 0 with count value 0AH

OR

8. a) (i) Write instructions to generate pulse for every 50µs from counter 0, frequency of 8253 is 2Mhz. (5)

(ii) How many modes do 8253 operate? Name all the modes.(5)

b) Give the significance of following signals and mention in which interfacing chip it is used, (10)

i) CS'

ii) C/D'

iii) DSR

iv) GATE 0

v) PC_0-PC_7

9. a) Explain Memory and I/O Interfacing in detail. (10)

b) Write 8279 control word format to initialize READ, WRITE and Display FIFO RAM, Keyboard display mode set. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2014 Digital Signal Processing

Set B

Time : 3 hrs
Total Marks: 100

1. a. Compute the eight-point DFT of the given sequence by using DIF-FFT algorithm.

$$x(n)=\begin{cases}1 & 0\le n\le 7\\ 0 & otherwise\end{cases}$$ (15)

b. Perform the circular convolution of the following sequences.

$x_1(n) = \{1,1,2,1\}$; $x_2(n) = \{1,2,3,4\}$ (5)

OR

2. a. Find $y(n) = x(n)*h(n)$ for the sequences $x(n) = \{3,-1,0,1,3,2,0,1,2,1\}$ and $h(n) = \{1,1,1\}$ using overlap add method. (12)

b. Determine the linear convolution via circular convolution of $x(n) = \{1, 3, 5, 7, 9, 11\}$ with $h(n)= \{4, 8, 16\}$. (8)

3. a. Design a Chebyshev filter for the following specifications using Bilinear Transformation. Assume T = 1 sec.

$$0.8\le\left|H(e^{j\omega})\right|\le 1 \quad for \quad 0\le\omega\le 0.2\pi$$
$$\left|H(e^{j\omega})\right|\le 0.2 \quad for \quad 0.6\pi\le\omega\le\pi$$

. (15)

b. Use Impulse invariance technique to obtain $H[z]$ for the analog transfer function

$$H(s)=\frac{2}{(s+1)(s+2)}$$

. (5)

OR

4. Obtain the direct form I, direct form II, Cascade and Parallel realization of the LTI system governed by the following equation .

$$y[n]=-0.1y[n-1]+0.2y[n-2]+3x[n]+3.6x[n-1]+0.6x[n-2]$$ (20)

5. Design an ideal high pass filter with the following frequency response using a Hamming window. Find the values of $h(n)$ for N=11. Find $H(z)$.

$$H_d(e^{j\omega})=\begin{cases}1 & for \quad \frac{\pi}{4}\le|\omega|\le\pi\\ 0 & for\ |\omega|\le\frac{\pi}{4}\end{cases}$$

(20)

OR

6. Determine the filter coefficients $h(n)$ obtained by frequency sampling for N = 7.

$$H_d(e^{j\omega})=\begin{cases}e^{-j(N-1)\omega/2} & 0\le|\omega|<\pi/2\\ 0 & otherwise\end{cases}$$

(20)

7. a. Explain input quantization error with an example. (10)

b. Consider a second order IIR filter and explain coefficient quantization error. (10)

OR

8. a. Illustrate zero-input limit cycle oscillations with an example. (10)

b. The output signal of an analog to digital converter is passed through a first order lowpass filter, with the following transfer function. Find the steady state output noise power due to quantization at the output of the digital filter.

$$H(z)=\frac{(1-a)z}{(z-a)} \; for 0<a<1$$ (10)

9. a. Draw the various blocks in the Harvard architecture and explain them in detail. (10)

b. Explain Least Mean Square algorithm in detail. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2015 Microcontroller and its Applications

Set B

Time : 3 hrs
Total Marks: 100

1. a) Write an assembly language program in 8051 to find the factorial of 5.(6)

   b) Explain the various addressing modes in 8051 with examples.(10)

   c) Write an ALP in 8051 to read data from port 1 and transfer the data to port 2 by masking the upper 4 bits. (4)

OR

2. a) Write 8051 ALP to count the number of 1's in EF. If the result is even, store 55 in memory location 4500. Else store AA. (10)

   b) Explain the architecture of 8051 with a neat diagram. (10)

3. (a) (i) After executing the instruction "MOV IP,#0C", discuss how the sequence in which the interrupts are serviced. Also explain about IE register of 8051 microcontroller. (6)

   (ii) Find the content of accumulator after executing the following instructions? (4)

   MOV A,#58H

   MOV R2,#03H

   LOOP: RL A

   DJNZ R2, LOOP.

   (b) Explain the various modes of timer in 8051.(10)

OR

4. a) Write 8051 ALP to transmit "ECE DEPT" serially to PC at 9600 baud rate. (10)

   b)(i) With a neat interface diagram, Explain how a 4x4 keypad is interfaced with 8051. (5)

   (ii) Assume that XTAL = 11.0592 MHz. What value do we need to load into timer register to create a time delay of 5 ms? Write a program using timer 0 to create a pulse width of 5 ms on P2.3. (5)

5. a) With a neat diagram, Explain the architecture of PIC 16CXX. (10)

   b) Write the arithmetic, logical and data transfer instructions used in PIC 16CXX microcontroller. (10)

OR

6. a) Explain the operation of timer 1 in PIC 16CXX module with a neat block diagram and mention the function of its associated register.(10)

   b) Explain the functions of all the ports available in PIC microcontroller. (10)

7. 7. a) In which timer module does the pre-scalar shared with watchdog timer? Explain the function of the appropriate timer with a neat block diagram. (10)

   b) (i)Write the various addressing modes in PIC microcontroller.(5)

   (ii) Given REG=1110 0110, W=0 and C=0, what will be the values in REG,W and C after executing the following instructions.(5) 1.RRF REG,W 2.RRF REG,f

OR

8. a) (i) Draw the interrupt logic diagram of PIC microcontroller. (5)

(ii) Brief the control registers used to control the interrupts in PIC microcontroller (5)

b) Give the significance of bus protocols used in PIC microcontroller. Explain in detail about I2C communication. (10)

9. a) Explain the operation of serial peripheral interface in PIC used for communicating with external peripheral devices. (10)

b) With a neat diagram explain how analog to digital converter is interfaced with PIC microcontroller. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2016 CAD for Electronics Engineers

Set B

Time : 3 hrs
Total Marks: 100

1. 1. Default value of net type is assigned as? [1]
   2. What statement and data type is used in dataflow & structural modelling with examples? [2]
   3. **Write a note initial and always block statement? [2]**
   4. **Implement a 1*4 demux using behavioral modelling techniques?** [5]
   5. Explain Floor planning and their techniques in detail. [10]

OR

2. 1. _____can be used for modelling both combinational and sequential. [1]
   2. **What is the difference between wire and reg? [1]**
   3. List all the net types and register data types in Verilog. [2]
   4. **Explain with suitable examples on data types and data operators in Verilog. [8]**
   5. With suitable example User defined primitives and User defined functions. [8]

3. 1. Depict the Simulink models for FM modulator and demodulator with a neat sketch. [10]
   2. Portray the Simulink model for sampling and reconstruction using sample-and-hold to measure the frequency response of the analog filters.[10]

OR

4. 1. Depict the general Simulink model for AM using subsystems. Portray the modulator and demodulator Simulink subsystem models. [12]
   2. Suppose x is a new variable, with the following MATLAB statement, [4]

      x = [-10: -1: -15; -2: 3]; what will be the result?

   3. What is the output of executing the following MATLAB code? [4]

```
Clear;
for i=1:5
for j=i:5
M(i, j) = i+j;
M(j, i)= M(i,j);
end
end
```

5. 1. Explain about constructors in MATLAB with an example. Also explain the steps in checking its output in command window. [15]
   2. Write a MATLAB class program to read from a file. [5]

OR

6.
1. Explain the concept of Binary search algorithm with a MATLAB class program. [15]
2. Explain about the features of Object Oriented Programming in MATLAB. [5]

7.
1. What is a cluster? [1]
2. Difference between waveform chart and waveform graph? [1]
3. What is array initialization? [2]
4. Differentiate array and cluster. [2]
5. Create a sub VI that takes a number representing Celsius and convert in to number representing Fahrenheit. Build a sub-VI for conversion of Celsius to Fahrenheit. Also list out the steps followed. [14]

OR

8.
1. Sketch FOR loop. [1]
2. Under what circumstances are for loop used? [1]
3. Differentiate between pretest mode and post-test mode. [2]
4. What is structure tunnel? [2]
5. Create a 1-D numeric array which consists of ten elements and rotate it ten times. For each rotation display the equivalent binary numbers of the first array element in the form of Boolean array. Also List down the steps to be followed. [14]

9. Explain about the concept of inheritance. Write a MATLAB class program with one superclass and two subclasses, considering the superclass as ‘Shape’ having a center position and color. Take the sub classes as circle and rectangle which should inherits the superclass functions and also calculates the area of its own shape. Also give the steps to find its output in command window. [20]

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2029 Embedded System Design

Set B

Time : 3 hrs
Total Marks: 100

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1. With a detailed diagram elucidate the embedded design life cycle with an example (20)

OR

2. a) Elucidate the working of stepper motor interfaced with 8051 microcontroller (10)

   b) Write an embedded c program to operate a SPDT relay connected with 8051 microcontroller. And Explain the operation with a neat block diagram.(10)

3. Design a paper vending machine by using embedded design life cycle flow with block diagram (20)

OR

4. a) How to interface two Buzzers' in microprocessor and microcontroller? Explain using diagrams (12)

   b) List and elaborate the handshaking signals of RS232. (8)

5. Explain the following:

   a.Task and task states b.RTOS with an example (20)

OR

6. a) With a neat block diagram, explain the Timer0 operation of 8051 along with the registers.(10)

   b) Discuss how DC motor is interfaced with 8051 microcontroller with necessary diagrams (10)

7. a) Differentiate synchronous and asynchronous communication (5)

   b) Explain the following: (15)

   a) SCI b) SPI c) SI

OR

8. a) What is the need for IDE in an Embedded Architecture? Discuss (10)

   b) Define protocols? Elucidate the types of protocols which is used in embedded communications. (10)

9. a) With a neat diagram explain the life cycle of task and task states (10)

   b) Mention the importance of scheduling in the RTOS system.(6)

   c) Elucidate Debug Kernels (4)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2038 Cellular Mobile Communication

Set A **Time : 3 hrs**
Total Marks: 100

1. a) Compare and contrast the various multiplexing techniques. (10)

   b) Give short notes on the advantages and disadvantages of micro cells in a cellular system. (5)

   c) Narrate on the fundamental propagation behavior of radio waves and its effects on propagation. (5)

OR

2. a) With a neat sketch explain the various digital modulation techniques. (15)

   b) Comprehend on the various effects of signal propagation. (5)

3. a) Comprehend on the various CSMA protocols. (10)

   b) What is interference? State the causes for interference? Brief on the various counter measures to overcome them? (10)

OR

4. a) Define handoff. Narrate on the various practical handoff considerations in mobile communication. (10)

   b) How do you increase the system capacity in the cellular mobile networks? (10)

5. a) With a neat ray diagram describe the process of mobile originated call and mobile terminated call. (10)

   b) Do cellular systems require handover? If so, with a neat sketch comprehend on the 4 possible handover scenarios in GSM. (10)

OR

6. a) IIlustarate on the system architecture of UTRAN. (10)

   b) Give an account on localization and calling in GSM. (10)

7. a) Enlist the different types of handover in satellite systems and explain them. (10)

   b) Using a neat block diagram describe the various earth orbits. (10)

OR

8. a) Explain on the various repetition of data. (10)

   b) Explain DAB with necessary diagram. (10)

9. a) Explain in detail about Dynamic Host Configuration protocol. (15)

   b) Compare Table driven routing and self driven routing. (5)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2044 Fundamentals of Wireless Communication

Set B

Time : 3 hrs
Total Marks: 100

1. a. Illustrate with diagram handoff scenarios at cell boundary during

   a. Improper handoff scenario
   b. Proper handoff scenario. (14)

   b. Define cell dragging. (3)

   c. Write notes on dwell time. (3)

OR

2. a. Explain in detail about low power, low cost radios. (16)

   b. What is the significance of the value Δ in handoff. (4)

3. a. If a transmitter produces 50 W of power, express the transmit power in units of (a) dBm and (b) dBW. If 50 W is applied to a unit gain antenna with a 900 MHz carrier frequency, find the received power in dBm at a free space distance of 100 m from the antenna. What is Pr (10 Km)? Assume unity gain for receiver antenna.

   (14)

   b. Brief on co-channel cells and frequency reuse (6)

OR

4. a. Determine the critical distance for the two-ray model in an urban microcell(ht = 10m,, hr = 3m) and an indoor microcell (ht = 3m, hr = 2m) for fc = 2GHz.

   (10)

   b. Give the transmit and receive signal model and explain the Doppler shift with necessary diagram. (10)

5. a. Consider an indoor wireless LAN with fc = 900 MHz, cells of radius 10 m, and nondirectional antennas. Under the free space path loss model, what transmit power is required at the access point in order for all terminals within the cell to receive a minimum power of 10 μW? How does this change if the system Frequency is 5 GHz? (10)

   b. Elaborate on free space path loss. (10)

OR

6. a. Explain how the complexity of signal propagation reduced using simplified path loss model. (14)

   b. Find the simplified multipath delay T_m for a two-ray channel model, when transmitter and receiver separation is relatively large d = 100 m, with ht = 10m and hr = 4m.

   (6)

7. a. Consider a set of empirical measurements of P_t/P_r given in the table below for an indoor system at 900 MHz. Find the path loss exponent γ that minimizes the MSE between the simplified model and the empirical dB power measurements, assuming that d_0=1m and K is determined from the free-space path gain formula at this d_0 Also find the received power at 150m for the simplified path-loss model with this path-loss exponent and a transmit power of 1mW.

Distance from transmitter	$M = P_t/P_r$
10 m	-70 dB
20 m	-75 dB

50 m	-90 dB
100 m	-110 dB
300 m	-125 dB

(17)

b. Define Q-function. (3)

OR

8. a. With proper equations explain the Impulse response of a time varying channel. (15)

b. Give the expression for simplified model of path loss (5)

9. a. Explain the capacity offered by an AWGN wireless channel in detail (14)

b. Consider a wireless channel where power fall off with distance follows the formula $P_t(d_0/d)^3$ for $d_0 = 10m$. Assume the channel has bandwidth B = 30 Khz and AWGN with noise PSD PSD $N_0/2$, where $N_0 = 10^{-9}$ W/Hz. For a transmit power of 1 W, find the capacity of this channel for a transmit – receive distance of 1 Km.

(6)

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14EC2046 Optoelectronics

Set B

Time : 3 hrs
Total Marks: 100

1. a. Give the relationship between electric and magnetic field in optical wave equation? (15)

   b. What are the conditions to obtain coherent wave trains required for the observation of Interference? (5)

OR

2. a. Elucidate about the optical phenomena of Luminescence. Explain different types of Luminescence. (5)

   b. Explain about Photoluminescence principle with the help of schematic diagram of energy levels. (10).

   c. What are the techniques followed to overcome the radiation losses in the construction of LED? (5)

3. a. Draw the structure of LED and explain its working principle of an electrolumniscence in detail. (15)

   b.For a GaAs/Glass LED interface n1=3.6,n2=1.5,then calculate the fractional transmission for an isotropic radiation inside the GaAs and the critical angle. (5)

OR

4. a. Obtain the expression for threshold condition for amplification in Laser cavity. (10)

   b. Discuss the theory of mode locking in Laser and explain about active and passive mode locking. (10)

5. a. Explicate the working principle of thermoelectric detector with necessary diagram. (10)

   b. Draw the equivalent circuit diagram of a photodiode with different modes and derive the external voltage equation. (10)

OR

6. a.Obtain the expression of photo conductive gain for a slab of photoconductive material. (10)

   b. Explicate the working principle of pyroelectric detector with necessary diagram. (10)

7. a. Discuss about the Birefringence and the Electro optic effect with application to phase modulation with necessary equations and diagram. (15)

   b. Draw the schematic illustration of acousto-optic modulation and explain the process of wave propagation ? (5)

OR

8. . a. Draw the schematic illustration of acousto-optic modulation and explain the process of

wave propagation ? (12)

b. Draw the schematic block diagram of an optoelecronic phased array antenna system. (8)

9. . a. Elucidate the techniques for fabricating waveguides with necessary diagrams. (10)

b. Brief about the principle forms of optoelectronic integration with their relative merits and demerits. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2050 Basics of Satellite Communication

Set A **Time : 3 hrs**
Total Marks: 100

1. (a) Mention the different services of the satellite systems with suitable applications. (6)

   (b) Derive the orbital period and velocity of the satellite with a neat sketch. (14)

OR

2. (a) i. What are the effects of orbital inclination of the satellite? (7)

   ii. Explain the coverage angle and slant range of orbital plane. (7)

   (b) Discuss in detail about frequency reuse techniques in satellite subsystem. (6)

3. (a) How a transponder hopping, polarization hopping and redundancy configuration made for up converter of the satellite subsystem? (10)

   (b) What are the commonly used low noise amplifier in earth station? Explain with a neat sketch. (10)

OR

4. (a) Explain what is meant by FDMA, and show how this differs from FDM, with a schematic. (10)

   (b) Briefly describe the ways in which demand assignment may be carried out in FDMA network. (10)

5. (a) Describe the general operating principles of a TDMA network. Show how the transmission bit rate is related to the input bit rate. (10)

   (b) Explain the need for reference burst and preamble and postamble in a TDMA system. (10)

OR

6. (a) Define and explain the terms carrier recovery, bit-time recovery, traffic data, frame efficiency and channel capacity in TDMA. (10)

   (b) Draw the super frame format of TDMA, Explain in detail about frame acquisition and synchronization process occur in it. (10)

7. (a) Explain the principle behind spectrum spreading and dispreading and how this is used to minimize interference in a CDMA system. (10)

   (b)Describe how signal acquisition and tracking are achieved in a DS/SS system with a neat sketch. (10)

OR

8. (a) Explain in detail about frequency hop spread spectrum system with a schematics. (10)

   (b)Write a short note on carrier recovery circuit with narrowband band pass filter and automatic frequency control loop in multiple access technique. (10)

9. (a) Explain how DBS operation is carried out with a neat diagram. (10)

   (b) Write a short note on (i) INTELSAT (ii) DOMSAT (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2068 VHDL

Set B

Time : 3 hrs
Total Marks: 100

1. a) Design ALU using VHDL. (15)

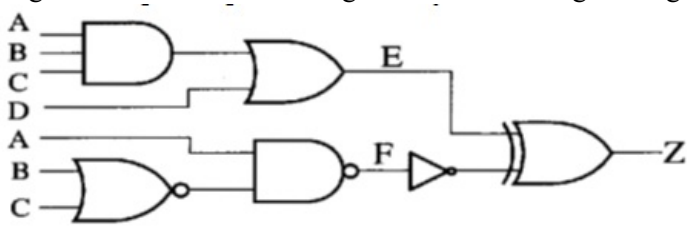
   b) Explain VHDL Operators. (5)

OR

2. a) Write Full adder structural model program using VHDL. Write all the component programs.(15)

   b) Write syntax for selected signal assignment statement. (5)

3. a) Write a VHDL Description of the following combinational circuit using Data flow modeling. Each gate has a 5 ns



   delay and the inverter has a 2 ns delay. (8)

   b) Design Updown counter using VHDL. (12)

OR

4. a) Explain all the delay models in signal assignment statement. (10)

   b) With example explain all types of wait statement. (10)

5. TYPE colour IS (white, yellow,Red,blue);

   TYPE word IS ARRAY(15 DOWNTO 0) OF bit;

   colour'left = -------- word'left = ----------

   colour'right = ------- word'right = ----------

   colour'high = --------- word'high = ----------

   colour'low = ---------- word'low =----------

   colour'length = --------- word'length = ---------- (10)

   Write RS and D flipflop VHDL programs. (10)

OR

6. a) Expalin VHDL funtion and procedure subprogram (10)

   b) Explain different object classes in VHDL.(10)

7. a) Design Mealy model sequential circuit using VHDL (15)

   b) Write syntax for VHDL FOR LOOP. (5)

OR

8. a) Design PISO and PIPO shift register using VHDL (15)

   b) Write short notes on VHDL Package. (5)

9. a) Design n bit adder using VHDL GENERICS statement (15)

   b) Write VHDL progarm for 4 bit SISO register (5)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2080 Communication Engineering

Set A

Time : 3 hrs
Total Marks: 100

1. Define and Derive the expression for Amplitude modulation, it's Power calculation & Current relation with necessary waveforms. (20 marks)

OR

2. a. Mention the need for modulation (6 marks)

b. An FM Wave is represented by the voltage equation,

$$e_{mod(t)}=35 \sin (15x10^6 t+7 \sin 8x10^4 t)$$

I. Determine the modulating and carrier frequency
II. Determine the carrier amplitude.
III. Determine the modulation Index
IV. Find the Carrier swing.
V. Determine the Frequency deviation.
VI. Calculate the bandwidth for FM if the number of sidebands are same as that of AM. (14 marks)

3. a. Discuss and derive in detail about a modulator that generates a DSB-SC signal with neat diagram**.** (15 marks)

b. Compare Linear and Non-linear modulation (5 marks)

OR

4. a. Explain in detail about obtaining Frequency Modulated signal indirectly. (8 marks)

b. Discuss about the Round Travis detector with necessary diagrams (12 marks)

5. State the disadvantages of Tuned radio frequency receiver and explain in detail about the method that overcomes the disadvantages of TRF. (20 marks)

OR

6. a. Derive and discuss about the SNR calculation for SSB-SC signal.(15 marks)

b. Briefly discuss about De-emphasis. (5 marks)

7. a. Plot the ASK, FSK and PSK modulated output waveform for the input 1101 (10 marks)

b. Explain in detail about the process of Pulse code modulation. (10 marks)

OR

8. a. Discuss in detail about Delta modulation. (14 marks)

b. Mention the process involved in MODEM functions (6 marks)

9. Discuss in detail about the scanning process of TV transmitter and receiver (20 marks)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2087 Micro Electro Mechanical Systems

Set A **Time : 3 hrs**
Total Marks: 100

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1. A) Explain the process of doping in detail. (10)

   B) Why is periodic table more important in determining the structure of atoms and molecules (10)

OR

2. A) What are the different silicon compounds. Explain its properties in detail (10)

   B) Determine the effect of resistance in silicon and relate how it is related to stress. (10)

3. Explain the process of diffusion in detail with relevant expressions (20)

OR

4. A) Explain how a structure is created by adding layer by layer on top of the substrate with neat diagrams (10)

   B) What are the major issues associated in surface micromachining. (10)

5. A) Compare and contrast the characters of wet etching and dry etching (10)

   B) Explain the working of photo transistor and photo diode with neat diagrams. (10)

OR

6. A) Explain the different etch stop techniques in bulk micromachining in detail with neat diagrams (12)

   B) Discuss in detail about different types of chemical sensors (8)

7. A) Explain the structure and function of beam resonator in detail (12)

   B) For a comb drive actuator , determine the voltage supply required to pull the moving electrode 10μm from the un stretched position of the spring. The spring constant k is 0.05 N/m. The comb drive is operated in air. The gap between the electrodes and the width of the electrodes are 2μm and 5μm. (8)

OR

8. Explain micro actuator. Explain the working principle of and the types of micro actuator. (20)

9. A) Discuss in detail about the 3D electromagnetic sensors with neat diagram (12)

   B) How DNA chip can be used in medical applications. Explain (8)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2090 Fundamentals of Electronics

Set A

Time : 3 hrs
Total Marks: 100

1. Discuss the Common emitter configuration of BJT and plot the dc characteristics. (10 marks)

   Explain in detail the formation of Extrinsic semiconductor and its characteristics (10 marks)

OR

2. A. Draw the energy band structure of a conductor, insulator and semiconductor? (6 marks)

   B. With neat sketch explain the characteristics, construction and working principle of PN diode. (14 marks)

3. Differentiate BJT and JFET (5 marks)

   Why UJT is called as a unipolar device. With neat sketch explain the construction, working principle of UJT. Also list out the applications. (15 marks)

OR

4. What are the ideal characteristics of op amp? Explain the OP-AMP applications with circuit diagram and output expressions. (20 marks)

5. A. Design a 2 bit digital adder circuit using logic gates and explain the procedure involved in it. (10 marks)
   B. Reduce the following logical expression using Boolean laws. Also prove that the number of gates used for constructing the system can be reduced by using Boolean law reduction. (10 marks)

   A'B'C' + A'BC' + AB'C' + ABC'

OR

6. A. With neat architecture diagram discuss the salient features of 8085 microprocessor. (15 marks)
   B. Mention the types of semiconductor memories and the use of it. (5 marks)

7. A. What are the requirements of a transducer? With neat diagram explain the working principle, advantages and applications of the passive transducer LVDT. (14 marks)

   Explain the necessity of signal conditioning unit with necessary diagram. (6 marks)

OR

8. A. Draw the block diagram of communication system and explain its operation. (10 marks)
   B. Find the height of the antenna required to transmit an audio frequency signal of frequency 5 kHz.Also discuss the need for modulation in detail.(10 marks)

9. Explain the schematic block diagram of optical fibre communication system. Also list the advantages and applications of optical fibre communication. (20 marks)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC2091 Electron Devices and Instrumentation

Set B

Time : 3 hrs
Total Marks: 100

1. Discuss the operation of PN diode characteristics in detail with its output wave forms?(20 Marks)

OR

2. Write the difference between half wave and full wave rectifier? Discuss the center tap transformer based full wave rectifier in detail.(20 Marks)

3. Draw the constructional diagram of LED and explain its operation in detail?(20 Marks)

OR

4. Write the advantages of optocoupler and explain its operation in detail with schematic diagram?(20 Marks)

5. Explain the operation of measurement of voltage and current using multimeter with all functional blocks.(20 Marks)

OR

6. What is mean by transducers and explain different types of transducers in detail with examples?(20 Marks)

7. Discuss the operation of digital voltmeter with its functional block diagram in electronic instrumentation.(20 Marks)

OR

8. Draw the detailed block diagram of digital data-acquisition system its operation in detail?(20 Marks)

9. How to test the radio receiver using the computer controlled system with its functional diagrams.(20 Marks)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3001 Statistical Digital Signal Processing

Set B

Time : 3 hrs
Total Marks: 100

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1. a.Show that the power spectrum of a WSS random process can be factorised as $P_x(z) = \sigma_0^2 H(z) H^*(1/z^*)$.(10)

   b.Explain the low pass filtering of white noise and find the power spectrum of white noise.(06)

   c.State the reason for the statement given: White noise is Strict Sense Stationary process.(04)

OR

2. a.Discuss in detail the significance of Parseval's theorem.(10)

   b.Mention the relation between Strict Sense Stationary (SSS) and Wide Sense Stationary (WSS) random process. Also describe why WSS is known as weakly stationary.(10)

3. a.Explain the following methods to measure be spectrum of long duration signals.(15)

   (i) ARMA model

   (ii) MA model

   b.What is the basic principle of the Welch method to estimate power spectrum?(05)

OR

4. a.Compare the performance measures for any three Non-parametric methods of spectrum estimation. (15)

   b.Define Periodogram. How DFT is used for its computation?(05)

5. a.Describe Levinson- Durbin recursion algorithm for solving the Toeplitz system of equations.(15)

   b.What is the overall computational complexity at each iteration of the LMS adaptive algorithm?(05)

OR

6. a.Derive the weight vector update equation for the LMS algorithm. Discuss in detail the convergence issues of the LMS algorithm.(15)

   b.State the two type variables of Kalman filter.(05)

7. a.Discuss in detail the steepest descent algorithmic steps and its limitations.(15)

   b.What is the significance of normalized LMS?(05)

OR

8. a.Derive the expression for Bartlett estimate and discuss the properties. (15)

   b.Design MA (1) process for the given auto correlation function $r_x(k) = 9\,\delta(k) + (0.5)^{|k|}$.(05)

9. a.What do you mean by multi-resolution analysis ? And explain how wavelet transforms can be used for this purpose.(10)

   b.Explain the process of decimation and interpolation with examples.(06)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3004 Hardware Description Languages

Set B **Time : 3 hrs**
Total Marks: 100

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1. a. Explain the various data objects of VHDL with examples. (15)

   b. What is the difference between Entity and Architecture?. Write the syntax for the entity. (5)

OR

2. a. Discuss in detail, the dataflow and structural modeling styles of VHDL with example programs? (15)

   b. List the design units of an entity and define them . (5)

3. a. Write a behavioral model, to design a Simple ALU. (10)

   b. Given the following declarations: (10)

   signal a,b,c : **std_logic**;

   type state_type is (idle,req,ack);

   signal state: state_type;

   indicate which of the following expressions is legal as a Boolean condition and if not, correct it.

   i. a **and not** b **and** c
   ii. a **and not** b **and** state=idle
   iii. a='0' **and** b **and** state = idle
   iv. a='1' **and** b ='0' **and** state = idle

OR

4. With appropriate example, explain the various operators of VHDL. (20)

5. a. Verilog provides many different operator types. Discuss them in detail. (15)

   b. Write a VHDL test Bench model for half adder circuit . (5)

OR

6. a. Write the general format of a test bench. (10)

   b. Write the equivalent process statement for the selected signal assignment statement. (5)

   type OP **is** (ADD, SUB,MUL,DIV)

   Signal OP_CODE: OP

   with OP_CODE **select**

   Z<= A+B **after** 10ns **when** ADD,

   A-B **after** 10ns **when** SUB,

   A*B **after** 10ns **when** MUL,

   A/B **after** 10ns **when** DIV;

   c. Develop a VHDL code for S-R flipflop model using concurrent assertion statement.(5)

7. What are the distinct components of a verilog module and explain the components with a simple example of an SR latch. (20)

OR

8. a. With a neat flow chart, illustrate the process involved in the basic computer-aided logic synthesis (10)

b. Explain the methods used in connecting ports to external signals with appropriate example. (10)

9. a. Describe the various parts of a UDP definitions and list the rules to be followed by both combinational and sequential UDP. (15)

b. List the differences between Tasks and Functions. (5)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3010 Data Compression Techniques

Set B

Time : 3 hrs
Total Marks: 100

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1. a) Bring out the various necessities for compressing the multimedia data. Also, point out the various check points to be noted during the compression process. (10)

   b) Encode the sequence A=[a, b, c, d, e, f, g] with the probability values [0.25, 0.15, 0.05, 0.1, 0.2, 0.2, 0.05] respectively using Shannon-Fano coding technique . (10)

OR

2. a) With neat diagram, illustrate the methodology of vector quantization techniques. (10)

   b) Comment briefly on the various models used for lossy compression techniques. (10)

3. a) Encode the sequence '…ghtghttghhhtgghtght….' using the LZ77 approach. Consider a window size of 13 with '6' as the size of the search buffer. (10)

   b) Encode the following sequence using digram coding technique. Assume a suitable initial dictionary with codewords. (10)

   'waswaswasyuiyuiyuiwyusiuwasyyyyuwassiuywa'

OR

4. a) Encode the sequence 'wabbawabbawabbawabbawooxwooxwoox' using the LZ78 algorithm. (10)

   b) With neat block diagram, explain the subband coding method for speech compression applications. (10)

5. a) Draw and explain the operation of channel vocoder with necessary mathematical equations. (15)

   b) Differentiate between voiced and unvoiced speech conditions. (5)

OR

6. a) With neat diagram, explain the code excited linear predictive coder with necessary mathematical equations. (15)

   b) Comment briefly on formant vocoders. (5)

7. With a numerical example, illustrate the process of SPIHT algorithm used for image compression. (20)

OR

8. How will you compress still images using JPEG algorithm? Support your answer with a neat block diagram. (20)

9. With neat block diagram, explain the operation of H.261 encoder used in video compression techniques. (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3011 Optical Networks and Photonic Switching

Set B

Time : 3 hrs
Total Marks: 100

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1. Explain the applications of various components used in the earlier generations of optical networks with necessary diagrams.

OR

2. Explain the operation of SOP and SWP Optical Isolators with its internal diagram.

3. a) Discuss the detailed operation of EDFA with neat diagram. (15)

   b) Explain the advantages of semiconductor optical amplifiers. (5)

OR

4. Explain the multiplexing scheme and the frame structure of SONET/SDH network.

5. Explain the concept of Enhanced HFC and FTTC in detail.

OR

6. a) Explain the wavelength routing PON architecture in detail. (12)

   b) State the applications of SONET/SDH (4)

   c) State the disadvantages of access networks over PPS networks (4)

7. Explain in detail about the equipment management scheme used to manage the configuration of optical networks.

OR

8. Elucidate the architecture of OADM with neat diagram.

9. Elucidate the various functions of OTDM network

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3012 Modern Digital Communication Techniques

Set B

Time : 3 hrs
Total Marks: 100

1. a. Derive the expression of PCM word size. Calculate it for a signal of peak value V_{pp} with a maximum of ±1% V_{pp} quantization distortion (8)

   b. Explain duobinary signaling of PCM data for the bit stream 101110 by taking reference bit-0 (12)

OR

2. a. Derive the expression for duo-binary PCM signaling transfer function. Plot and illustrate the features of it (12)

   b. Draw and explain the block structure of baseband detection system (8)

3. a. Given a bit stream 1011011001, draw the following PCM waveforms (12)

   i. NRZ-L ii. NRZ-M iii. Bi-Φ-L iv. Bi-Φ-S

   b. Plot and compare the spectral features of various PCM schemes (8)

OR

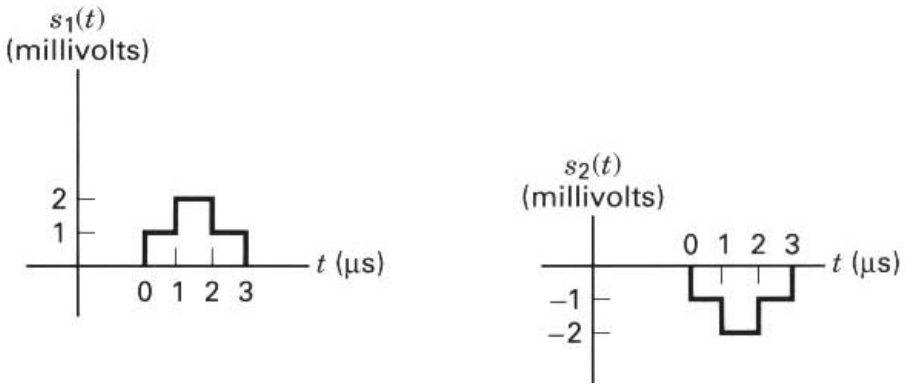
4. a. Explain the A-law and μ-law of companding with graphical structure (10)

   b. List out all the parameters used to choose a PCM waveform (5)

   c. Draw the block diagram of formatting and transmission of baseband signals (5)

5. a. Derive the expression for maximum SNR of matched filter (15)

   b. Following figure has signals with AWGN are received by a matched filter. Given $N_0=10^{-12}$ W/Hz. Compute the bit error probability (5)



OR

6. a. For two antipodal signals $s_1(t)$ and $s_2(t)$, draw the equivalence of matched filter and correlative filter (6)

   b. Explain raised cosine filter and plot its characteristics (14)

7. a. Brief the theory of channel characterization with its transfer function (7)

   b. With neat block diagram, explain decision feedback equalizer (13)

OR

8. a. Brief the M-ary signaling schemes and compare their error performance (10)

   b. Compare the working process and the features of matched filter and correlative receiver configurations (10)

9. a. With block schematic and spectrum, explain in detail the concept of multicarrier modulation technique (15)

   b. What are the properties of an estimator? (5)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3013 Wireless Communication Networks

Set B

Time : 3 hrs
Total Marks: 100

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1. a) Explain Diversity-Multiplexing Trade-offs (13)

   b) Write about Space-time modulation (7)

OR

2. Write short notes with necessary diagrams on the following wireless services (5x4=20)

   a)Broadcast

   b)Paging

   c)Cellular telephony

   d)Wireless Local Area Networks

   e)Ad hoc networks and Sensor networks

3. Draw and explain spatial multiplexing and BLAST Architectures (20)

OR

4. a) Explain the methods of spectrum allocation (10).

   b) Draw and explain the basic wireless communication systems (10)

5. a) Explain the architecture of 3GPP wireless network. (12)

   b) Write the features and challenges of 4G network. (8)

OR

6. a) Explain the operation of the stream rotation (10)

   b) Mention the functions of IEEE 802.11 WLAN physical layer (10)

7. a) Mention the advantages and disadvantages of 3G wireless networks. (7)

   b) Draw and explain the architecture of UMTS. (13)

OR

8. a) Discuss polarization diversity and frequency diversity (10)

   b) Explain fading and intersymbol interference with necessary diagrams. (10)

9. a) What about diversity and its necessity with proper sketch (10)

   b) Explain shadowing with necessary diagram (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3019 Digital System and ASIC Design

Set A

Time : 3 hrs
Total Marks: 100

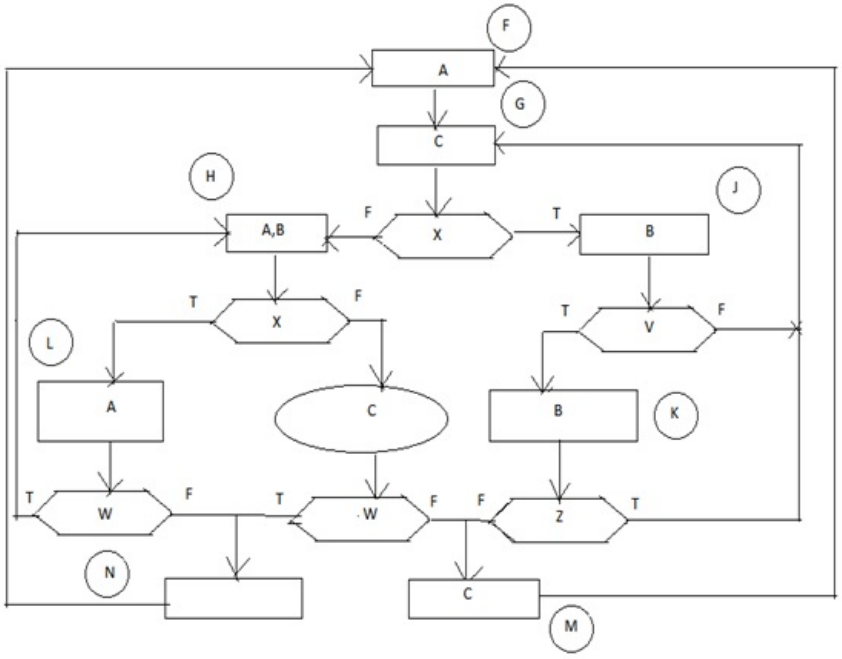
1. Design a sequence detector using JK FF that produces an output 1 whenever the sequence 1010 is detected. (20)

OR

2. Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output Z.

   The output Z=1 if x_1 changes from 0 to 1, Z = 0 if x_2 changes from 0 to 1, and Z=0 otherwise. Realise the circuit using D FFs. (20)

3. Given the ASM Chart in fig. find the design equations for the state variables and for the outputs. Assume that the design uses a minimum number of D FFs. (20)



OR

4. **a).** Explain the Actel ACT 1 architecture with neat diagram. And also explain the Actel ACT timing model with diagrams. (12)

   b). Implement the following Boolean functions using a PAL. (8)

   $W(A,B,C,D) = \sum (1,3,4,6,12)$

   $X(A,B,C,D) = \sum (7,8,9,10,11,12,13)$

   $Y(A,B,C,D) = \sum (0,2,3,4,5,6,7,8,12)$

   $Z(A,B,C,D) = \sum (1,2,8,12,13,14,15)$

5. a).Draw and explain the following interconnect architectures. (15)

   i). Altera MAX 5000

   ii). Altera FLEX

   iii). Xilinx EPLD

   b).Explain the design flow for the Xilinx implementation of the halfgate ASIC. (5)

OR

6. a)..Explain hierarchical nature of an EDIF (Electronic Design Interchange Format) file. (5)

   b).Explain EDIF (Electronic Design Interchange Format) files for an inverter. (15)

7. a). Explain the following programming technologies. (12)

   i). Antifuse

   ii).EPROM

   b). Explain CFI (CAD Framework Initiative) design with an example. (8)

OR

8. a).Explain Xilinx LCA interconnect architecture with neat diagrams. Also find the delay in the path. (15)

   b).Explain priority encoder with diagram . (5)

9. a).Implement Vending Machine Controller using DFFs and PLA. (12)

   b).Explain Xilinx Spartan II Configurable logic block in detail. (8)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3020 CMOS VLSI Design

Set A

Time : 3 hrs
Total Marks: 100

1. (a) Derive the threshold voltage equation of a MOS Structure. (12)

(b) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A=10^{16}$ cm^{-3}, polysilicon gate doping density $N_D=2x10^{20}$ cm^{-3}, gate oxide thickness t_{ox}=500Å, and oxide interface fixed charge density $N_{ox} = 4x10^{10}cm^{-2}$ (8)

OR

2. a) Discuss in detail about the operation of MOS transistor in different operating regions with various terminal voltages.(14)

b)Design the following by using CMOS Logic. (6)

(i) $F= \overline{((A.B) + (C.D))}$ by using CMOS Logic.

(ii) $Z= \overline{((A.B.C) +D)}$ by using CMOS Logic.

3. a) Explain the DC and Transfer characteristics of CMOS inverter and derive the expression for output voltage in various operating regions.(14)

b)Draw the stick diagram and layout for 2-input CMOS NAND Gate.(6)

OR

4. a) Find the Propagation delay of a 0.25µm CMOS Inverter whose supply voltage is 2.5V, the normalized ON resistance of NMOS and PMOS transistors equal 13 kΩ and 31kΩ respectively. The W-to-L ratios of the transistors to be 1.5 for NMOS and 4.5 for the PMOS. The C_L for NMOS and PMOS is to be 6.1fF and 6.0fF.

(8)

b) Explain the concept of computing the capacitances of CMOS Inverter. (12)

5. a)Describe in detail about Pass transistor Logic, its energy drawn from the power supply and Differential Pass transistor Logic. (10)

b) Discuss in detail about Dynamic CMOS Logic with its basic principles and important properties.(10)

OR

6. (a) Explain the all the concepts involved in Robust and Efficient Pass-Transistor Design. (16)

(b) Draw the function Z= A.B+ C.D using Domino CMOS Logic. (4)

7. a) Explain in detail about multiplexer based latches and master slave positive edge-triggered register

using multiplexers. (10)

b) Explain in detail about True Single-Phase Clocked Register. (10)

OR

8. a) With neat diagram explain about Carry-Bypass Adder. (10)

b) Explain with neat diagram about sense amplifier based register.(10)

9. a)Explain in detail the signal integrity issues in Dynamic CMOS Design. (14)

b) Describe the effects of cascading the dynamic n-type blocks. (6)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3021 Analysis and Design of Integrated Circuits

Set A **Time : 3 hrs** **Total Marks: 100**

1. (a) Describe in the input output characteristics of an amplifier and derive the relationship with is non linear function and estimate the need of large signal analysis (7)

b)Derive the source follower gain using small signal model and obtain its small signal equivalent (14)

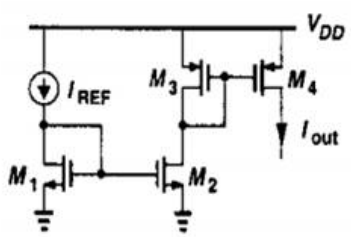
OR

2. In detail explain the operation of the common source amplifier and obtain the following parameter

1. Large signal model
2. Small signal model
3. Output Impedance
4. Input Resistance

3. (a) Describe in the input output characteristics of an differential amplifier and derive the relationship and estimate the need of large signal analysis (10)

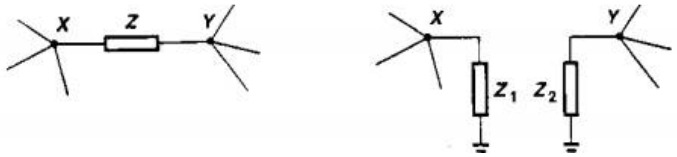
(b)Derive the current in the M4 transistor of the given circuit, explain the operation of the circuit in detail (10)



OR

4. (a) With biasing of a current mirror obtain the output resistance and the input output characteristics of the current mirror. (10)

(b) Derive the miller effect for the floating impedance of the given elements and an amplifier (10)

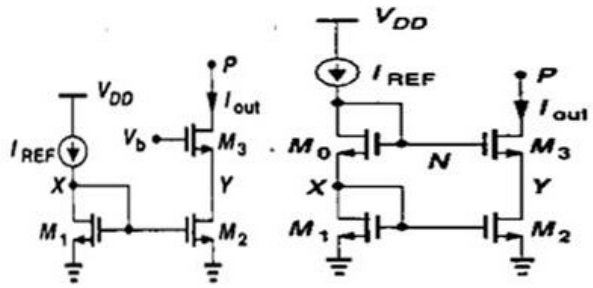


5. a) Describe in the PSRR of differential amplifier and derive the relationship with is non linear function and estimate the need of PSSR (8) (b) Derive the noise in two stage operational amplifier and using thermal noise and flicker noise obtain its total noise equivalent circuit (12)

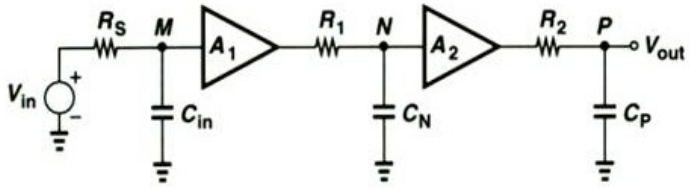
OR

6.

(a) In detail explain the operation of the following current mirror (10)



(b)Derive the associated poles with the nodes for the given circuit. (10)



7. (a)Obtain the positive and negative temperature voltagefor the temperature independent reference circuits (14)

(b) Give an issues in the operational amplifier with respect to the speed and noise of the system and give its significance (6)

OR

8. (a) Describe in the PSRR of differential amplifier and derive the relationship with is non linear function and estimate the need of PSSR (8) (b) Derive the noise in two stage operational amplifier and using thermal noise and flicker noise obtain its total noise equivalent circuit (12)

9. (a) Derive the noise in the single stage amplifier, derive the noise in common drain and common source amplifier (16)

(b)What are the issues in the noise and speed of the circuit transients on reference voltage and currents (4)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3022 VLSITechnology

Set A

Time : 3 hrs
Total Marks: 100

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1. a.Explain in detail about the method of depositing a thin layer over a substrate using molecular beam epitaxy. (16)

   b.What are the different deposition techniques for growing thin layers? (4)

OR

2. a.Explain the method of Czochralski Crystal Growing. (12)

   b.How will you convert a metal grade silicon to electronic grade silicon? (8)

3. a.What are the different types of lithography available in semiconductor IC fabrication?(5)

   b.Explain in detail about the various steps involved in lithography that adopts UV rays?(15)

OR

4. a.What is a back scattering effect in electron beam lithography? (4)

   b.Explain the lithography method adopted to overcome the back scattering effect that happens in e-beam lithography. (16)

5. a.Explain few common atomic diffusion models in a solid using a simplified two dimensional crystal structure. (10)

   b.Explain in detail about rapid thermal annealing. (10)

OR

6. a.Explain about the diffusion in Polysilicon. (10)

   b.Explain about the diffusion in SiO_2.(10)

7. a.Explain in detail about the various effect in the diffusivities of Boron, Phosphorus, Arsenic and Antimony. (20)

OR

8. a.List out the desired properties of the metallization for integrated circuits. (10)

   b.List out the possible metallization choices for integrated circuits. (6)

   c.Show how the various types of simulation are interrelated with each other in fabrication.(4)

9. a.Explain about the thin film growth using a high vacuum chamber Physical Vapor Deposition. (12)

   b.List out the post metal processing steps. (8)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3023 Solid State Device Modeling and Simulation

Set A

Time : 3 hrs
Total Marks: 100

1. a) For the n channel MOSFET obtain the small signal model.Also specify the necessity of small signal modelling. (14)

   b) "**Miniaturization is the need of the hour"**. Justify and comment on the parameters affected by scaling (6)

OR

2. a)Calculate the V_T of an MOS Capacitor where we deposit a high –k gate deielectric,HfO_2, whose relative dielectric constant is 25,on a novel p type semiconductor whose electron affinity is 4eV, band gap is 1.5eV, relative dielectric constant is 10 ,and intrinsic concentration is $10^{12}cm^{-3}$. The gate is made of a metal whose work function is 5eV, gate oxide thickness is 100Å and N_A is$10^{18}cm^{-3}$ and that has a fixed charge of 5x $10^{10}qC/Cm^2$.At V_T, what are the electron and hole concentrations at the oxide-semiconductor interface and deep in the substrate? Sketch the band diagram normal to the surface at V_T (12)

   b) Draw the different energy band diagrams (at equilibrium, when accumulation, inversion and strong inversion) and approximate distribution of electric charge, electric field and electrostatic potential in ideal MOS capacitor in inversion for p channel base (n substrate) (8)

3. a)Using Pah-Sah model, the drain current of long channel MOSFET can be obtained only theoretically. Prove with appropriate equations (10)

   b) Calculate the V_T of a Si- P Channel MOS transistor for an n^+ -polysilicon gate with silicon dioxide thickness = 50Å ,N_d = 1x 10^{18} cm^{-3} and a fixed charge of 2 x $10^{10}qC/Cm^2$.Is it an enhancement or depletion mode device? What B dose is required to change V_T to 0V? Assume a shallow B implant. (10)

OR

4. a) Ellaborate on the influence of a) Channel length modulation b) Source and drain resistance c) Ballistic transport on the drain current and threshold voltage of a MOSFET (6)

   b) Give a detailed account of the exact I-V model that brings out the drain current of a long channel MOSFET. Also highlight the limitations of this model (14)

5. a) State Mathiesen's rule.What are the factors that contribute to the effective mobility of the charge carriers? (6)

   b) Derive the drift and diffusion current of a long Channel MOSFET using Compact surface potential model. (8)

   c) Differentiate between compact surface potential and charge controlled compact MOSFET models(6)

OR

6. a) What impact does mobility of the charge carriers have on the drain current of the MOSFET ? Explain with required expressions(12)

   b) How is it possible to increase the carrier velocity from source to drain without affecting the length of the channel ? (8)

7. a).Define transit time and obtain an expression for the same for MOSFET. (6)

   b).What are capacitive coefficients? Calculate the capacitive coefficients of a MOSFET (14)

OR

8. a). Using impedance field method ,obtain the expression for thermal noise in MOSFET (10)

b). List the steps involved in the simulation of the mobility models of MOSFET using COMSOL Multiphysics 4.4 (10)

9. a) Why are high frequency models used ? Obtain the drain current and source current of a MOSFET using HF model ? (12)

b) Ellaborate on the different Surface potential models (8)

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14EC3024 Low Power VLSI Design

Set B

Time : 3 hrs
Total Marks: 100

1. a). A 32 bit off-chip bus operating at 3V and 300 MHz clock rate is driving a capacitance of 20pF/ bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus? (5)

   b).Derive an expression for dynamic power dissipation in a CMOS inverter due to charging and discharging of capacitance. (10)

   c). Explain basic Principles of low power design. (5)

OR

2. a). The chip size of a CPU is 20mm x 45 mm with clock frequency of 800MHz operating at 2.4 V. The length of the clock rouing is estimated to be twice the circumference of the chip. Assume that the clock frequency is routed on a metal layer with width of 1.8µm and the parasitic capacitance of the metal layer is 3Ff/μm^2. What is the power dissipation of the clock signal? (5)

   b). Discuss the variation of short circuit current of a CMOS inverter for input signal slope and output load capacitance. (10)

   c) Derive an expression which relates static probability and frequency. (5)

3. a).Explain the techniques to use logic encoding to achieve low power consumption. (15)

   b).Explain gate reorganization to reduce power in logic level. (5)

OR

4. a).Explain in detail various Power Reduction Techniques in Clock Networks. (15)

   b). How to take precautions to avoid floating node in CMOS circuits to reduce power consumption. (5)

5. a. Explain different types of leakage current in deep sub-micrometer transistor.(15)

   b. Explain power management in architectural level with an example. (5)

OR

6. a) Show how parallelism has been used to improve computation throughput of high performance digital systems. (8)

   b). Explain how glitches can be reduced in array multiplier by using delay balancing. (12)

7. a). Explain with neat diagrams single and double edge triggered FFs. (10)

   b) Write notes on flow graph transformation. (10)

OR

8. a). Derive an expression which relates the conditional probability and frequency. (10)

   b). Explain about gate level power analysis. (10)

9. Explain in detail about the low power SRAM architecture. (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3029 Speech and Audio Signal Processing

Set B

Time : 3 hrs
Total Marks: 100

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1. a.What are the types of phonemes in American English? Specify with at least one example in each case.(12)

   b.Why Cognitive Effects are important in Judging Audio Quality? Draw the block diagram of the basic approach in the development of cognitive corrected PAQM model and explain.(08)

OR

2. a.Categorize the speech sound by changing vocal tract shapes and explain with an illustration.(12)

   b.For a 20 KHz, 16-bit sampling audio signal, how many bytes are used in 5 seconds? (04)

   c.A sound file has a storage size of 440 KBytes with the resolution of 16 bit. How long is the play time, if it is played at a 22 KHz rate?(04)

3. a.Explain the following pre echo control strategies(10)

   i. Bit reservoir,
   ii. Window switches,
   iii. Gain modification, and
   iv. Switched filter banks

   b.Compare the eight channels Discrete Fourier and Discrete Cosine Transform filter bank.(10)

OR

4. a.Discuss in detail the steps involved in Psychoacoustic Model of MPEG 1 audio coding.(15)

   b.Draw the coder and decoder block diagram of lossy audio coding based on sub-band coding and psychoacoustic models.(05)

5. a.Draw the block diagram of Homomorphic filter and explain about the characteristic systems.(16)

   b.Give the expression for pitch by Cepstral method.(04)

OR

6. a.With neat block diagram explain the STFT realized by bank of modulators and low-pass filters.(16)

   b.Discuss about the properties of Cepstrum.(04)

7. a.Derive the expression for the LPC coefficients by autocorrelation method.(16)

   b.Why the LPC is often referred to as inverse filtering? State the reason.(04)

OR

8. a.With illustration describe the design considerations of M-band filter banks for Audio Coding.(15)

   b.List highly desirable filter bank characteristics for effective audio coding.(05)

9. Discuss about the adaptive codebook with the help of schematic diagram of a Code-Excited Linear Prediction coder. And also explain the excitation generation using the stochastic code book in the CELP model.(20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3030 Biological Signal Processing

Set A **Time : 3 hrs**
Total Marks: 100

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1. a) Illustrate the methodology of measurement of ENG signals with neat diagrams. (10)

   b) What is EMG? Explain the characteristics of EMG signals along with the acquisition procedure. (10)

OR

2. a) Describe the sequence of operations during the rhythmic activity of the human heart? (10)

   b) Draw a sample ECG signal and bring out the specific nature of each segment. Also, specify the ECG acquisition procedure using Einthoven's triangle. (10)

3. a) Bring out the technical concepts of power spectral density function and cross spectral density functions.(15)

   b) How will you use the smoothing methodology for variance reduction in periodogram of input signals?(5)

OR

4. a) How will you estimate the parameters of Moving Average (MA) models? (15)

   b) Explain the direct method of estimation of parameters in ARMA models (5)

5. a) Comment briefly on the methodology of pattern classification for biosignal processing applications.(10)

   b) What are the various distance measures used in supervised classification techniques? (10)

OR

6. a) Differentiate supervised and unsupervised pattern classification methodologies. (5)

   b) Deduce the step-by-step procedure of a simple cluster seeking algorithm used for unsupervised classification applications. (15)

7. a) How will you use minimum distance classifier for solving the pattern classification problem? (15)

   b) Comment briefly on any one of the types of data reduction techniques (5)

OR

8. a) Describe any one of the probabilistic classifiers used for pattern classification applications (15)

   b) How can you incorporate the wavelet concepts for bio signal processing applications? (5)

9. Draw the architecture of back propagation neural network. With mathematical expressions, derive the weight adjustment rules used for training the network. Suggest suitable ways by which the network can be used for classifying the bio signals. (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3031 Medical Image Processing

Set A

Time : 3 hrs
Total Marks: 100

1. (a) Describe the following data processing components in single-crystal scintillation camera (i) position encoding matrix (ii) summation and deflection amplifier and (iii) pulse summation circuit. (12)

   (b) Explain the principle of computed tomographic (CT) imaging. List three reasons why contrast resolution is improved in CT imaging compared with conventional radiographic imaging. (8)

OR

2. (a) With regard to Positron Emission Tomography explain its principle, advantages over similar methods, limitation and recent developments. (12)

   (b) Compare various types of collimators. (8)

3. (a) Discuss the various components of image noise. (12)

   (b) List the image characteristics that influence image clarity. Determine the geometric unsharpness for a radiographic procedure with a 2 mm focal spot, object-to-receptor distance of 25 cm and source-to-receptor distance of 100 cm (8)

OR

4. (a) Discuss on subject and motion unsharpness. Determine the geometric unsharpness for a radiographic procedure with a 2 mm focal spot, object-to-receptor distance of 25 cm and source-to-receptor distance of 100 cm. (12)

   (b) Explain how in digital fluoroscopy, the automatic brightness control unit maintains a constant brightness on the output screen of the image intensifier. (8)

5. With necessary diagram explain the pulsing and signal acquisition scheme used in the following pulse sequences: Spin-echo, Carr-Purcell-Meiboom-Gill and Inversion recovery (20)

OR

6. (a) Discuss the following with respect to sensitive point method: (i) data acquisition (ii) practical implementation and (iii) limitations. (9)

   (b) If it takes 300 msec to obtain a single voxel by using a sensitive-point technique, how much time is required to obtain five slices with a matrix size of 256 × 256? (3)

   (c) Explain the phenomenon of free induction decay. (8)

7. (a) Discuss how the parameters TR,TE,T1 are selected in spin echo sequence to maximize the tissue contrast. (8)

   (b) A spin-echo pulse sequence has a TE of 100 msec. A new pulse sequence begins 800 msec after the MR signal or echo is received. Three signal averages and 256 phase encoding steps are used. Find the total image acquisition time. (4)

   (c) Write short notes on MR Spectroscopy. (8)

OR

8. (a) Compare the various presentation modes in Ultrasound imaging. (5)

   (b) Short notes on ultrasound imaging artifacts. (8)

   (c) With necessary diagram describe the components of Ultrasound B-mode imaging system. (7)

9. (a) Discuss on Radon transform with regard to image reconstruction from projections. (10)

(b) With necessary diagram explain the digital implementation of convolution back-projection algorithm. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3042 RF System Design

Set A **Time : 3 hrs**
Total Marks: 100

1. a. What are the key components of a mobile phone? (5)
   b. Draw the block diagram of a generic RF system (7)
   c. Compute the intrinsic wave impedance, phase velocity, and wavelength of an EM wave in free space and a PCB material (with $\varepsilon_r = 4.6$) for the frequencies 30 MHz and 3 GHz. Compare and justify the results (8)

OR

2. Explain the construction and working of the following.
   a. Chip resistors (10)
   b. Chip capacitors (10)

3. a. Design a micro-strip LPF with $Z_{IN}=Z_L=50\Omega$. The other specifications are as follows. f_c=3GHz; equi-ripple of 0.5 dB; rejection of at least 25dB (at approximately $1.5f_c$). Assume a dielectric material that offers a phase velocity of 60% of the speed of light (10)
   b. Draw the micro-strip line structure of a band pass filter (4)
   c. Brief the theory of surface-mounted inductors (6)

OR

4. a. What is the need for HF modeling of semiconductors? (4)
   b. Explain the physical properties of semiconductors and derive the expressions for minority and majority carrier concentration (16)

5. a. With energy band diagram, explain Schottky contact and derive the expression for its junction capacitance (10)
   b. Explain the construction and working of PIN diode (10)

OR

6. Explain the following BJT large signal models
   a. Ebers-Moll model (13)
   b. Gummel-Poon model (7)

7. a. Explain the concept of constant VSWR circles in RF amplifier design (10)
   b. Design a balanced broadband amplifier using 3dB and Wilkinson power couplers (10)

OR

8. a. Explain the design process of Quartz oscillators (8)
   b. Explain the design of dielectric resonator oscillators (12)

9.	a.	Explain the characteristics and concepts of mixer design with frequency domain considerations	(13)
	b.	With neat circuit diagram explain the working process of double-balanced active mixer	(7)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3046 Communication Network Security

Set B **Time : 3 hrs** **Total Marks: 100**

1. a. Define Cryptosystem. Explain it with suitable diagram. (8)

b. Explain the concept of Public key and Private key used in cryptography. What is the advantage of having two separate keys? (6)

c. Compare between Symmetric cryptography and Asymmetric Cryptography. (6)

OR

2. a. Explicate about Blowfish Algorithm with supporting sketches. (12)

b. What is digital signature? Discuss digital signature algorithm in detail. (8)

3. a. Describe the Diffie-Hellman key exchange algorithm. (8)

b. Alice and Bob want to establish communication using the Diffie –Hellman key exchange protocol, with q = 71 and a primitive root α = 7.

(i) If Alice has private key XA = 5, what is Alice's public key? (4)

(ii) If Bob has private key XB = 12, what is Bob's public key? (4)

(iii) What is the shared secret key? (4)

OR

4. a. Enumerate the properties of Hash Function. (6)

b. Explicate SHA in detail with necessary diagrams. (14)

5. a. Illustrate your perception on key management in IPSec. (5)

b. Represent the ISAKMP header format with a neat sketch and necessary description. (15)

OR

6. a. Show the IPSec document overview with a neat sketch and describe briefly. (6)

b. Portray about the IPSec AH and the scope of AH authentication. (14)

7. a. Elucidate in detail about SSL architecture with necessary diagrams. (12)

b. Portray the Web security considerations briefly. (8)

OR

8. a. Explicate over SET – (Secure Electronic Transaction) overview, key features and participants. (10)

b. Portray the concept of Dual signatures implied in SET with necessary diagrams. (10)

9. Portray your perception over the concepts of trusted systems, data access control and Trojan horse defense methodologies. (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3047 Communication Network Routing Algorithms

Set B

Time : 3 hrs
Total Marks: 100

1. i. Why do we need hierarchical routing? (4 marks)

   ii. Why do cellular calls always go through home MTSO? (4 marks)

   iii. Why does Mobile IP require tunneling? (2 marks)

   iv. What are te routing protocol requirements? (4 marks)

   v. What are the problems and solutions with Distance Vector Routing? (6 marks)

OR

2. i. What are the various security protocol choices? (5 marks)

   ii. What is crankbank? Is crankbank useful to improve the QoS?(5 marks)

   iii. Comprehend on Dijkstra's algorithm with a suitable example? (10 marks)

3. i. Enlist the advantages and disadvantages of proactive and reactive routing algorithm?(5 marks)

   ii. Give an account on tier routing in large scale packet radio networks? (15 marks)

OR

4. i. Explain DSDV in detail. (12 marks)

   ii. Comprehend on the routing in large sized packet radio networks? (8 marks)

5. . i. Define hand off. Using a suitable ray diagram explain the various hand off techniques? (10 marks)

   ii. Using a case study comprehend on the routing process in cellular networks? (10 marks)

OR

6. i. Compare and contrast BGP and EGP. (8 marks)

   ii. Comprehend on RIP. (12 marks)

7. i. Comprehend on the architecture and working pattern of packet radio networks? (10 marks)

   ii. Why quasi hierarchical routing is need in networks? Mention its significance? (5 marks)

   iii. Comprehend on the advantages and disadvantages of tier and hierarchical routing? (5 marks)

OR

8. Suppose a router obeyed the flodding rule that it forwarded an incoming packet to every interface (except the one it arrived on) if the packet was not a duplicate.

   a. Assume that the routers do not see any part of the packet header except the destination address. The simplest way to know if a packet is duplicated is to store every packet, and comparing incoming packets with stored ones. If the mean packet length is 500 bytes, and the router receives 200 multicast packets per second, how much storage does the router consume every second? (4 marks)
   b. If the router decides to discard packets that are more than 10 minutes old, how much storage does it need? (4 marks)
   c. How many packets are stored on average? (3 marks)
   d. If comparing entire packets takes 200microseconds, how much time does it take to compare an incoming packet with every stored packet? (4 marks)
   e. Suppose the router computes a 10 byte checksum for a packet, and stores checksums instead of packets, using checksum to compare packets. If computing a checksum takes 200 microseconds, and

comparing checksums takes 2 microseconds, What is the gain in space and time of this approach over storing entire packets? (5 marks)

9. i. Using a case study comprehend on the routing process in TORA routing algorithm? (14 marks)

ii. Compare TORA and SSR routing algorithms. (6 marks)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3048 Embedded Sensor Networks

Set A **Time : 3 hrs**
Total Marks: 100

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1. a. Develop a sensor network model for forest fire detection in siruvani hills. Use appropriate sensor nodes. (10)

   b. Individual components of sensor node play a vital role in achieving energy efficiency. Justify. (10)

OR

2. a. Suggest suitable timing technique for sensor network. (10)

   b. Can conventional TCP be used for wireless sensor networks? Why? (10)

3. a. Why traditional MAC protocols are not suitable for sensor networks. What are the reasons for power wastage in MAC? (10)

   b. Explain co-ordinated sleeping and data transmissions in S-MAC. Bring out its merits. (10)

OR

4. a. How S-MAC improves latency caused by periodic sleep? (10)

   b. What is the use of location information in embedded sensor networks? (10)

5. a. Find the feasibility of IEEE 802.15.4/Zigbee technology for wireless sensor network design. (10)

   b. Why GPS is not suitable for many applications of wireless sensor network? How is it overcome? (10)

OR

6. a. Explain the various Distance estimation methods. (10)

   b. How location is estimated by Trilateration? (10)

7. a. Discuss the two types of database organization. Bring out the pros and cons of each. (10)

   b. Case i) Last year average rainfall of Tamil Nadu.

   Case ii) Forest fire detection

   Mention the type of data aggregation performed in the above cases. Justify. (10)

OR

8. a. Mention the useful sleep states in the sensor node architecture. (10)

   b. Formulate a State transitioning policy to achieve energy efficiency. (10)

9. Explain Bluetooth piconets. Discuss its implications for wireless sensor networks. (20)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3049 Mobile Communication Networks

Set B **Time : 3 hrs**
Total Marks: 100

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1. a. Describe the steps carried out in global mobile system ,when a call is terminated by mobile user (10)

   b. Narratethe issues involved inNetwork Dimensioning (10)

OR

2. a. Explain in detail about the principle of Frequency division channel access method (10)

   b. What are theplanning strategies adoptedtoallocate the resources for networking (10)

3. Name the different types of hand off mechanisms? Explain in detail (20)

OR

4. a. Discuss the features of IS -136 with frame structure (10)

   b. With frame format , explain the functions of AMPS protocol (10)

5. a. With the reference architecture ,explain general packet Radio service System (10)

   b. Discuss the important Features and Services in GSM (10)

OR

6. a. List the steps carried out in GSM ,when a call is initiated by mobile user (10)

   b. Discuss the services of 3G mobile networks. Compare the features of W-CDMA with CDMA 2000 (10)

7. Draw the frame structure and explain the features of MAC layers in IEEE 802.11 standard (20)

OR

8. a. Why CSMA/CD is not suitable for wireless networks? Explain in detail about CSMA/CA with a flow chart (10)

   b. Describe the DCF access scheme in IEEE 802.11 with handshaking (10)

9. a. Discuss the important issues involved in wireless security (10)
   b. Describe the features of secure routing in wireless networks (10)

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14EC3053 Design of Semiconductor Memories

Set B **Time : 3 hrs**
Total Marks: 100

1. **a. Describe with necessary diagrams, different types of application specific SRAM. (16)**

   b. List the advantages of SOI technology over bulk silicon technology in the design of RAM. (4)

OR

2. **a Differentiate between hard error and soft error and discuss how soft error occurs in DRAM. (16)**

   b. Justify the usage of trench capacitor in the design of high density DRAM. (4)

3. **a. Describe with necessary diagrams, different types of application specific DRAM. (16)**

   b. **Define "grow back" phenomenon in PROM cell structure. (4)**

OR

4. **a. With suitable figures, explain how program, read and erase operations are performed in a Flash memory. (14)**

   b. Mention and explain the programming element used for PROMs developed by Actel Corporation. (6)

5. **a. Explain in detail about parametric testing in memories. (10)**

   b. Compare the state transition diagrams of 2 cells in fault free and faulty state assuming the fault to be inversion coupling fault when the aggressor moves from 1 to 0. (10)

OR

6. **a. Discuss about various Functional Testing Algorithms. (16)**

   b. With state diagram, indicate how a 0 to 1 transition fault occur in a memory cell. (4)

7. **a. Discuss about the reliability issues of PROM and EPROM memory. (10)**

   b. Explain about radiation hardening design issues (10)

OR

8. **a. Explain about SRAM failures modes and mechanisms. (10)**

   b. Discuss about single-event phenomenon in memories. (10)

9. **a. Discuss in detail about various experimental memory devices. (16)**

   b.Compare FRAM with EEPROM with respect to its operating characteristics. (4)

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14EC3056 Analog VLSI Design

Set B **Time : 3 hrs**
Total Marks: 100

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1. (i) Explain the MOS characteristics in all the regions of the device (10)

   (ii) What are the different scaling factors in MOSFET device. How do you scale the device? Explain with suitable expressions. (10)

OR

2. (i) How will you determine the input and output characteristics in comparators. Explain the static characterization of op amp. (10)

   (ii) Explain the operation of MOSFET device in detail (10)

3. (i) How will you estimate the total charging and discharging time in dual slope ADC with neat diagrams and relevant expressions (15)

   b) How will you apply charge scaling technique in DAC. Explain (5)

OR

4. (i) Discuss the current scaling technique in D/A convertors with neat diagrams. (10)

   (ii) How will you detect a digital word '101' when Vmax is '1V' and the input voltage is 0.7V using a high performance ADC. Explain (10)

5. (i) Discuss the dynamic characteristics of ADC (5)

   (ii) b) How the time difference is directly proportional to voltage. Explain the serial slope method ADC with neat necessary diagrams. (15)

OR

6. (i)How will you replace a resistor using a switch capacitor circuit? Justify with relevant expressions. (12)

   (ii) Design a current amplifier with suitable expressions (8)

7. (i) Design a two input difference amplifier and explain the condition to make the transistor to work in saturation region. (12)

   (ii) Design a LPF for the given transfer function $Z(s) = \frac{2s^3 + 2s^2 + 2s + 1}{2s^2 + 2s + 1}$ (8)

OR

8. (i) Design an integrator using Switched Capacitor Circuit.(10)

   (ii) Design a high gain amplifier with relevant expressions (10)

9. Design a two stage open loop comparator with relevant expressions. (20)

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14EC3063 Nanoscale Devices and Circuit Design

Set B **Time : 3 hrs** **Total Marks: 100**

1. a). Derive the MOSFET I_d vs V_{ds} characteristics for long channel and short channel devices. (15)

   b).Explain important High-κ dielectrics used for sub 100 nm technology MOSFETs. (5)

OR

2. a). Discuss 2D MOS Electrostatics by using 2D Poisson equation. (15)

   b). Discuss various Biaxial s-Si MOSFET structures with neat diagrams. (5)

3. Explain how the electron concentration profile changes with the following parameters in double gate MOS device. (20)

   i. Gate voltage effect

   ii. Semiconductor thickness effect

   iii. Gate oxide thickness effect

OR

4. Derive the expressions for the I-V characteristic of the ballistic MOSFET assuming that the electron gas is degenerate and nondegenerate. (20)

5. Derive the I-V characteristics of a silicon nanowire MOSFET for the following. (20)

   i). nondegenerate carrier statistics.

   ii).degenerate carrier statistics.

OR

6. a).Discuss the subband energy Vs wavevector (k_1) of a heterostructure quantum well. (10)

   b).Explain the energy band transitions in heterostructure quantum well. (10)

7. a).Discuss the tunneling through a potential energy barrier with the junction with the following interfaces.

   i). Metal-Insulator interface.

   ii). Metal-Semiconductor interface.

   iii).Metal-Insulator-Metal interface. (10)

   b).Discuss the physics of MOSFET in the presence of scattering. (10)

OR

8. a). Discuss various Ge-MOSFET structures for nanoscale applications. (10)

   b). Explain single electron transistor concepts with neat diagrams. (10)

9. a).Discuss the power and performance analysis of different modes of FinFETs based NAND gates. (12)

   b).Discuss the operating principle of a bistable Resonant Tunneling diode logic gate. (8)

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14EC3071 Digital Image Processing

Set A **Time : 3 hrs** **Total Marks: 100**

1. a) Elucidate the various functional blocks of digital image processing (15 marks)

   b) Distinguish between digital image and binary image. Give suitable example to each type of images.(5 Marks)

OR

2. a) Describe in detail about the elements of visual perception with neat diagram.(10 Marks)

   b) Describe briefly about Image sampling and Quantization. (10 Marks)

3. a) Describe in detail about the elements of image processing system. (10 Marks)

   b) Explain the various ways of sensing and acquiring an image. (10 Marks)

OR

4. a) Discuss the image smoothing filter with its model in the spatial domain.(14 Marks)

   b) Take any two popular image processing tools and make a relative comparison of different option available in such tools.(6 Marks)

5. a) Differentiate spatial domain filtering and frequency domain filtering. (4 Marks)

   b) Explain image degradation model /restoration process in detail. (16 Marks)

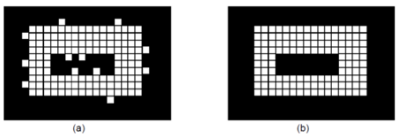
OR

6. a) Explain the principal of a linear and nonlinear filter used for image smoothening. (10 Marks)

   b) Discuss about the different noise distribution model in detail.(10 Marks)

7. a. Propose a morphological procedure to clear the edge artifacts of the image given in (a) such that the image in (b) is obtained. Clearly state the structuring element(s) and number of iterations that you would use in your procedure.

   (10 Marks)



   b. How do we perceive colour? Why red, green and blue are generally accepted as primary colours which when mixed in appropriate proportions generate other colors? (10 marks)

OR

8. Explain the following morphological algorithms: (10+10 Marks)

   a) Region filling b) Extraction of connected components

9. Write short notes on (10+10 Marks)

   i. Watershed Segmentation ii. Use of motion Segmentation

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3072 Advanced Digital Signal Processing

Set A

Time : 3 hrs
Total Marks: 100

1. 1. a. Determine whether x[n] = 5 sin[2n] is periodic, and if it is, find the fundamental period. (3)

b. Determine whether the discrete system, y[n] = 0.25 x[n-1] +0.5x[n] + 0.25 , where y[n] and x[n] are respectively the output and input sequences is (3+3+1)
i)Linear/Non-linear , ii)Time variant / Time invariant (iii) Causal/Non causal

c. Let $x^2_{ev}[n]$ & $x^2_{od}[n]$ denote, respectively the even and odd parts of a square-summable sequence x[n]. Prove the following result: (10)

$$\sum_{n=-\infty}^{\infty} x^2[n] = \sum_{n=-\infty}^{\infty} x_{ev}^2[n] + \sum_{n=-\infty}^{\infty} x_{od}^2[n].$$

OR

2. a. Test whether the signal $x[n] = e^{j2\pi n/3} + e^{j3\pi n/4}$ is periodic or not and if the signal is periodic, calculate the fundamental period. (4)

b. If

$$x[n] = \begin{cases} n^2 + n & -3 \le n \le 3 \\ 0 & otherwise \end{cases}$$

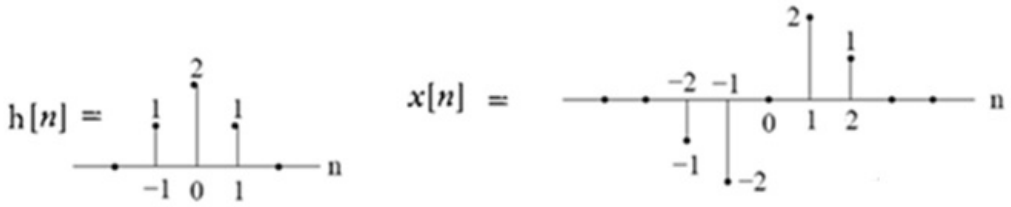
Plot the sequence x[n] and hence find (3+2+3)

(i) 2 x[2-2n]

(ii) x[n+1] +x[n-1]

(iii) x[3-n/4]

c. A system has an impulse response h[n] and input x[n] as shown in figure below. (8)



Determine the response of the system. Is the system causal? Why?

3. a. Determine the 4 point circular convolution of the two length- 4 sequences g[n] and h[n] given by g[n]={1,2,0,1} ; h[n] = {2,2,1,1} . Hint: Use the graphical method of circular convolution.

(5)

b. Compute the 4-point DFT of the sequence (10)

$$x[n] = \begin{cases} 1, & 0<=n<=3 \\ 0, & \text{otherwise} \end{cases}$$

by using the decimation-in-frequency FFT algorithm.

c. Prove that IDFT can be calculated using DFT algorithm. (5)

OR

4. a. The following signals are defined on the interval n = 0, 1, 2, 3. (10)

$x_1[n] = (1/2)^n$ $x_2[n] = (-1)^n$.

Compute the 4 point circular convolution using DFT. Use matrix method for solving DFT.

b. Obtain the response of an LTI system whose impulse response h[n] = {2,1} and input x[n] = { 1,2,3} using DIT FFT algorithm. (10)

5. a. Design a linear phase FIR band pass filter to pass frequencies in the range $w_{c1} = 0.35\pi$ radians/sample to $w_{c2} = 0.48\pi$ radians/sample using rectangular window by taking 5 samples of the window sequence. (10)

b. Using minimum number of multipliers, realize the cascade structure of (5)

$$H(z) = \left(\frac{1}{5} + \frac{1}{2}z^{-1} + \frac{1}{5}z^{-2}\right)\left(\frac{1}{7} + \frac{1}{4}z^{-1} + \frac{1}{7}z^{-2}\right)$$

c. Write the algorithm for software implementation of digital Butterworth IIR filter design. (5)

OR

6. a. Derive the expression of bilinear transformation and hence deduce the relationship between analog frequency W and the digital frequency w. Also explain the concept of frequency warping. (10)

b. Obtain the direct form I, direct form II and Cascade realization of the LTI system (6)

$$H(z) = \frac{1 + 3z^{-1} + 2z^{-2}}{1 + 0.375z^{-1} - 0.09z^{-2} - 0.015z^{-3}}.$$

c. Write the steps to design an FIR filter using frequency sampling technique. (4)

7. a. Convolve the signals $x_1[n] = \delta[n] - \delta[n-2] + \delta[n-3]$ and $x_2[n] = 2\delta[n-1] + \delta[n-2] - \delta[n-3]$. Use the tabular column method for discrete convolution and verify the result using Z transform method.(10)
b. Derive the time-domain and frequency-domain expression for the Decimation operation of factor D. (10)

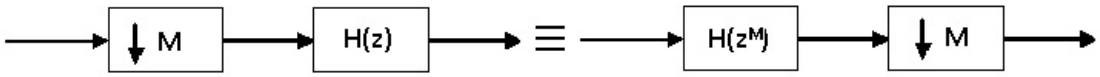
OR

8. a. The sampling rate of a signal x[n] is to be reduced, by decimation, from 96 kHz to 1 kHz. The highest frequency of interest after decimation is 450 Hz. Design the specification of filters LPF1,

LPF2 and LPF3 for a three stage decimation as shown in fig. below with an overall pass band ripple of $\delta p = 0.01$ and stop band deviation $\delta s = 0.001$. (10)

b. Explain with block diagram the implementation of Audio-Sub band Coding and Decoding system. (10)

9. a. Prove the following Cascade Equivalence. (10)



b. Explain how a fraction of sampling time (kT_S/L, k and L are integers) phase shift can be effected for the input signal multi-rate signal processing. (10)

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End Semester Examinations - Nov-Dec 2015 Exams

14EC3073 FPGA Design for Industrial Applications

Set B **Time : 3 hrs** **Total Marks: 100**

1. a. What are the different data types in VHDL? Explain briefly about scalar data type? (10)

   b. With an example, discuss about different data operators in VHDL (10)

OR

2. a. Design a 4 bit parallel adder using structural modeling in VHDL (10)

   b. Write a Test Bench program for 1*4 Demultiplexer (5)

   c. For the given signal object performs the following operation and obtain the result. (5)

   Signal a: std_logic_vector (6 downto 0);

   A <= "1001010"

   A sll5; A ror3; A sra3; A rol4; A (3 downto 0) & "111"

3. a. Develop the VHDL code for 4*1 Multiplexer using Block statement? (4)

   b. Explain the two kinds of subprograms in VHDL with examples? (6)

   c. Draw the Physical design flow and briefly explain each stage in the design flow? (10)

OR

4. . a. Explain the different types of Loop statements in VHDL with examples? (8)

   b. Compare the ASIC Design and FPGA Design (any five points) (4)

   c. Explain the Named association and Positional Association in the structural modeling with examples? (6)

   d. What is the simulation action of the following VHDL statement? (2)

   clk <= not clk after 10ns

5. a.What are the different types of ASIC? Explain briefly about Semicustom ASIC? (13)

   b. Explain the Halfgate ASIC Design in various design software tools? (7)

OR

6. a. Explain the various Programming Technologies used in ASIC? (12)

   b. Draw the Xilinx FPGA Design flow and briefly explain the process flow with the significance of each stage in the design flow? (8)

7. a. Draw the Altera FLEX architecture (Logic array Block) and explain its working? (7)

b. What is meant by FPGA Partitioning? (3)

c. Explain the Xilinx LCA interconnect architecture with neat diagram? (10)

OR

8. . a. Explain the Xilinx XC3000 and XC5200 Configurable Logic Blocks with neat diagram? (10)

b. List out the differences between the CPLD and FPGA. (3)

c.Draw the Actel ACT interconnect architecture and explain its working? (7)

9. . a. Mention the advantages of using PLD devices (2)

b. Draw the ASM chart for a Mealy state machine sequence "111" with ASM transition table? (8)

c. Implement the following Boolean functions using the PAL device. (10)

$W(A, B, C, D) = \Sigma m(2, 12, 13)$

$X(A, B, C, D) = \Sigma m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$Y(A, B, C, D) = \Sigma m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$Z(A, B, C, D) = \Sigma m(1, 2, 8, 12, 13)$

Wishing you All the Best

Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - Nov-Dec 2015 Exams

14EC3078 Real Time And Embedded Control Automation

Set B

Time : 3 hrs
Total Marks: 100

1. (a) What are the types of an embedded systems? (4)

   (b) Describe the functional components involved in embedded system application development? (12)

   (c) What are the typical characteristics of an embedded system? (4)

OR

2. (a) Elaborate on various design process and metrics that is to be optimized in an embedded system design. (12)

   (b) Write down the various steps involved for the conversion of assembly code into machine implementable code. (8)

3. (a) List the procedure for selection of ADC and design to be used in an embedded system. (4)

   (b) Describe the generation of pulse width modulation signals in software and hardware. (16)

OR

4. Explain the various methods by which the stepper motor is interfaced to a microcontroller. Also discuss the drive system.

5. (a) With example, illustrate the Java based embedded system design. (8)

   (b) Discuss the role of petrinets and draw a petrinet model for scheduling process. (12)

OR

6. (a) Discuss the importance of finite state machine (FSM) in embedded system design. (8)

   (b) Write a pseudo code program to describe Traffic Light System operation. (8)

   (c) Write short notes on simulation of an embedded system. (4)

7. (a) Elaborate on different task states with an example. (8)

   (b) Discuss how Priority Inversion problem is handled by Real time kernel in RTOS. (12)

OR

8. With neat sketch, illustrate the different methods of handling interrupt services in RTOS environment.

9. (a) What are the RTOS System Level Functions and Semaphore Related Functions. (8)

   (b) Explain about the Mailbox and Message queue related functions available in UCOS-II. (12)

Wishing you All the Best