Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Sub. Code:** | **14EC3054** | **Duration :** | **3hrs** |
| **Sub. Name:** | **HARDWARE DESIGN VERIFICATION TECHNIQUES** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Analyze the importance of functional verification and discuss in detail about the various functional approaches. | CO1 | 12 |
| b. | Differentiate Testing and verification with neat explanation. | CO1 | 8 |
| (OR) | | | | |
| 2. | a. | With neat waveforms describe in detail about Event-driven and Cycle-based simulation. | CO1 | 14 |
| b. | What is the need for code reviews? | CO1 | 6 |
| 3. | a. | Identify the metrics that thoroughly the verification suite exercises the source code being verified. | CO1 | 6 |
|  | b. | Recognize the issue tracking system in which issues are repeatedly reported loud and clear. | CO1 | 8 |
|  | c. | Predict the metrics that are related with the functional verification that other productivity metrics. | CO1 | 6 |
| (OR) | | | | |
| 4. | a. | Distinguish in detail about different types of coverage that is used by the verification suite. | CO1 | 14 |
|  | b. | Conclude that the evolutionary system only addresses the lack of owner ship of grapevine system. | CO1 | 6 |
| 5. | a. | With neat diagram explain in detail about levels of verification. | CO1 | 12 |
|  | b. | What is first-time success, how a design is verified, and which test benches are written. Discuss in detail about the verification plan. | CO2 | 8 |
| (OR) | | | | |
| 6. | a. | Using test vectors, verifying a design is cumbersome and they are hard to interpret and difficult to specify correctly. Find a suitable method for the design to verify it and observing the response. | CO1 | 12 |
|  | b. | The test bench approach requires a similar configuration of the design, use the same abstraction level for the stimulus and response. Determine the appropriate test bench approach. | CO2 | 8 |
| 7. | a. | Discuss in detail about verifying the output using visual inspection of response , simulation results and by minimizing the sampling. | CO2 | 15 |
|  | b. | Analyze in detail about features to testcases. | CO2 | 5 |
| (OR) | | | | |
| 8. | a. | All design teams have informal systems to track issues and ensure their resolutions.Find the issues and check the functionality of the design. | CO3 | 15 |
|  | b. | Verify in detail about self checking test benches. | CO2 | 5 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Ilustrate in detail about eVC architecture with DUT and eVC,BFMs and Monitors. | CO3 | 15 |
|  | b. | Describe briefly about Reusable Verification.Components(eVCs),Clocks ,Events,DUT Signals and Agent Details. | CO3 | 5 |