Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Code** | **14EC3037** | **Duration :** | **3hrs** |
| **Sub.Name** | **DSP ARCHITECTURE AND PROGRAMMING** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Find the number of multiplications required to perform convolution of two sequences of length 8 each by (i) direct method (ii) indirect method using FFT. | CO1 | 10 |
| b. | Explain briefly the difference between von Newmann architecture and Harvard architecture for the computer. Which architecture is preferred for DSP’s and why? | CO2 | 5 |
| c. | Using direct form and its equivalent structure for FIR filter, explain the structurepreferred for high speed real time signal processing.. | CO1 | 5 |
| (OR) | | | | |
| 2. | a. | Discuss the advantages of Digital Signal Processing. | CO3 | 5 |
| b. | Explain with block diagram, the subband processing system that processes M subbands. | CO3 | 10 |
| c. | Find the number of stages and twiddle factors required for the computation of 512 point DIT-FFT | CO2 | 5 |
| 3. | a. | Write a C5x assembly level program for the implementation of FIR filter using MAC instruction. (Assume h[n] = { 3,4,5}, x[n] = {1,2,3,2,1 } ) | CO3 | 14 |
|  | b. | Explain the Direct and Indirect Addressing feature of TMS320C5x Processor. | CO2 | 6 |
| (OR) | | | | |
| 4. | a. | Draw the table showing the content of the instruction pipeline of TMS320C5x processor & the content of ARP, AR6,TREG0,PREG,ACC registers when each of the sequence of 1-word instructions of the following program is executed. Initial content of memory locations 60h = 10h, 61h = 3h & 62h = 6h.  **ADD \*+**  **SAMMTREG0**  **MPY \*+**  **SQRA\*+, AR2** | CO1 | 10 |
|  | b. | Explain how delayed branch/call instructions are superior to the undelayed branch/call instructions. | CO2 | 10 |
| 5. | a. | Discuss the features of the Dual Operand Addressing Unit of TMS320C54x Processor. | CO2 | 12 |
|  | b. | Write short notes on the Bus Structure of TMS320C54x Processor. | CO1 | 8 |
| (OR) | | | | |
| 6 | a. | Explain the Functional units in the Data Paths of TMS320C6x architecture. | CO1 | 12 |
|  | b. | Compare the TMS320C6x assembly programs to implement MAC operation with and without parallel instructions. | CO1 | 8 |
| 7. | a. | Write short note on pipelining feature of TMS320C54X processor. | CO2 | 10 |
|  | b. | Explain the VLIW architectural feature of TMS320C6X CPU. | CO3 | 10 |
| (OR) | | | | |
| 8. | a. | Discuss the use of Shadow register for Input and Output registers in each of the subunits of ADSP-21xx processor. | CO2 | 10 |
|  | b. | Discuss the multi precisioncapability and ALU Saturation Mode of ADSP-21xx processor. | CO2 | 10 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Draw the internal architecture of TMS320C5XCPU and explain each of its constituent functional blocks ( CALU , PLU & ARAU ). | CO1 | 12 |
|  | b. | Explain the following Data Move instructions with examples.  BLDP, BLPD, BLDD. | CO1 | 8 |

ALL THE BEST