Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Sub. Code:** | **14EC3025** | **Duration :** | **3hrs** |
| **Sub. Name:** | **CAD FOR VLSI CIRCUITS** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. |  | List different fabrication process in VLSI and Write its impact on physical design in detail. | CO1 | 20 |
| (OR) | | | | |
| 2. | a. | Draw ‘Y’ chart for VLSI design tools and explain all the models in detail relevant to Computer aided design. | CO2 | 14 |
| b. | List the difference between full custom design and semicustom design. | CO2 | 6 |
| 3. |  | Describe the depth first search algorithm and explain the same with the sample pseudo code for CAD VLSI design. | CO2 | 20 |
| (OR) | | | | |
| 4. | a. | Narrate the importance of breadth first search algorithms in Computer aided design for VLSI Design. | CO2 | 10 |
| b. | Define Vertex and Edge in Graph representation. | CO2 | 10 |
| 5. | a. | Write short notes on Simulation. | CO1 | 10 |
| b. | Explain in detail about Logic Synthesis and verification. | CO1 | 10 |
| (OR) | | | | |
| 6. |  | Write the Shannon expression and explain the binary discuss diagram(BDD) in detail. | CO1 | 20 |
| 7. |  | Describe the different design styles present in partitioning in VLSI and explain the same in detail. | CO1 | 20 |
| (OR) | | | | |
| 8. | a. | Define placement. Discuss different levels of placement present in CAD VLSI with relevant diagrams. | CO2 | 10 |
| b. | What is mean by Design rule check in VLSI and explain the DRC in detail. | CO1 | 10 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Define multi chip modules. Explain the need of MCM in VLSI. | CO2 | 10 |
| b. | Explain the physical design cycle of MCM using neat flow diagram and its applications. | CO2 | 10 |

ALL THE BEST