Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Code** | **14EC3024** | **Duration :** | **3 hrs** |
| **Sub. Name** | **LOW POWER VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | | Marks |
| 1. | a. | Discuss the need for Low Power VLSI chips and basic Principles of low power design. | CO1 | | 7 |
| b. | Discuss about gate level power analysis. | CO1 | | 8 |
| c. | The chip size of a CPU is 20mm x 35 mm with clock frequency of 600MHz operating at 2.8 V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock frequency is routed on a metal layer with width of 1.0µm and the parasitic capacitance of the metal layer is 3Ff/µm2. What is the power dissipation of the clock signal? | CO3 | | 5 |
| (OR) | | | | | |
| 2. | a. | Compute the transition density and static probability of y= ab + c  given P (a) = 0.2, P (b) = 0.3, P(c) = 0.4 , D(a) = 1, D(b)=2, D(c) = 3 | CO1 | | 14 |
| b. | Explain about architectural level power analysis. | CO1 | | 6 |
| 3. | a. | Apply network restructuring concepts to the circuit Y= AB+CD+E. | CO3 | | 6 |
|  | b. | Discuss the architecture of Bus invert encoding with neat diagram. Analyze its performance in terms of efficiency. | CO1 | | 14 |
| (OR) | | | | | |
| 4. | a. | Derive the expressions forthe power and delay of an inverter chain using transistor sizing. | CO1 | | 8 |
|  | b. | Discuss the concepts of equivalent pin ordering with an example. | CO1 | | 6 |
|  | c. | Show how State machine encoding reduce power in the digital circuits. | CO1 | | 6 |
| 5. | a. | Apply Shannon decomposition theorem in the Precomputation Logic Technique to reduce power with an example. | CO3 | | 10 |
|  | b. | Apply delay balancing concepts to array multiplier to show the switching activity of the circuit is reduced. | CO1 | | 10 |
| (OR) | | | | | |
| 6. | a. | Apply various techniques to clock networks of processor chips to reduce Power. | | CO3 | 14 |
|  | b. | How to take precautions to avoid floating node in CMOS circuits to reduce power consumption? | | CO1 | 6 |
| 7. | a. | Explain different types of leakage current in deep sub micrometer transistor. | | CO3 | 10 |
|  | b. | Show how parallelism has been used to improve computationthroughput of high performance digitalsystems. | | CO3 | 10 |
| (OR) | | | | | |
| 8. | a. | Write notes on flow graph transformation. | CO1 | | 6 |
|  | b. | Explain in detail the power and performance management techniques to reduce power in architecture leveland also one technique to reduce power in digital filters. | CO3 | | 14 |

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|  | | **Compulsory:** |  |  |
| 9. | a. | Explain in detail the organization of a RAM and also explain the operation of 6T MOS static RAM memorycell. | CO2 | 10 |
|  | b. | Explain the methods of reducing power in Writer Driver circuits and Sense Amplifier circuits of SRAMcore. | CO2 | 10 |

ALL THE BEST