Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May – 2017**

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| **Code :** | **14EC2072** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALYSIS AND DESIGN OF DIGITAL IC** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Justify that the resistance of the two metal slabs shown in figure is same. | CO2 | 2 |
| b. | Design CMOS inverter as an amplifier. | CO1 | 4 |
|  | c. | Illustrate the SPICE simulation of a step input applied to an inverter driving a capacitive load with the given process parameter values Vtn = 0.767 V, Vtp = -0.938 V, βn = 4.04 x 10-4, βp = 3.48 x 10-4, VDD = 5 V, CL = 0.5pF and hence distinguish between analytical delay model and empirical delay model. | CO2 | 14 |
| (OR) | | | | |
| 2. | a. | Mention the parameters of p and n type devices in an inverter to obtain same rise and fall time. | CO3 | 2 |
| b. | Define Channel region in MOSFET with diagram. | CO1 | 4 |
| c. | With neat diagram explain the different steps involved in the fabrication of NMOS transistor and define threshold voltage. | CO1 | 14 |
| 3. | a. | Mention the disadvantage of Pass transistor logic and indicate a solution for the same. | CO3 | 3 |
|  | b. | Draw the block diagram of NORA logic design style. | CO1 | 3 |
|  | c. | With diagram analyze the different issues that occur in dynamic logic design style and provide suitable solutions for the same. | CO3 | 14 |
| (OR) | | | | |
| 4. | a. | Draw the block diagram of np-CMOS logic design style. | CO3 | 3 |
|  | b. | With equation explain about the short circuit power dissipation in CMOS circuits. | CO3 | 3 |
|  | c. | Design a 2 input OR gate using complementary CMOS, pseudo NMOS and pass transistor logic design styles and reason out which design style is efficient. | CO1 | 14 |
| 5. | a. | List the types of power dissipation in CMOS circuits. | CO3 | 3 |
|  | b. | In an IC, mention the fundamental component that is integrated. | CO1 | 1 |
|  | c. | Design and analyze Footless domino logic design style, list the challenges and provide a solution for the same. | CO2 | 16 |
| (OR) | | | | |
| 6. | a. | Draw the block diagram of NORA logic design style. | CO1 | 5 |
|  | b. | Design F=ABC using np-CMOS logic design style and explain its operation. | CO1 | 15 |
| 7. | a. | Differentiate between static and dynamic memory based on their storage time and clocking. | CO2 | 2 |
|  | b. | Draw the block diagram of MUX based positive latch. | CO1 | 2 |
|  | c. | Design and explain the operation of positive edge triggered register with timing diagram and analyze the demerits of the design. | CO1 | 16 |
| (OR) | | | | |
| 8. | a. | With block diagram differentiate between combinational and sequential logic circuits. | CO2 | 2 |
|  | b. | With timing diagram explain negative latch | CO1 | 2 |
|  | c. | Design clocked version of SR latch and explain its operation. | CO1 | 8 |
|  | d. | With neat diagram, illustrate the bistability principle and explain an application where it is used. | CO3 | 8 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Design a pipelined datapath using C2MOS latches and mention the advantages of C2MOS latches over C2MOS registers. | CO1 | 10 |
|  | b. | Design an AND gate using true single phase clocked approach and explain its operation. | CO1 | 10 |

ALL THE BEST