Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | List the various Data typesin VHDL. | CO1 | 10 |
| b. | Design a 4X1 Multiplexer circuit using VHDL structural modeling. | CO2 | 10 |
| (OR) | | | | |
| 2. | a. | For the given signal object perform the following operation and obtain the result.  Signal a: std\_logic\_vector(7 downto 0);  **A<= "11011011"**  A sll2 ;  A ror3;  A sra 4;  A rol 3;  A(4 downto 0) &"111"; | CO1 | 10 |
| b. | If the declarative part in the architecture of a half adder is as below    component XOR2    port (X,Y:in BIT;z: out BIT);    end component    component AND2    port (L,M:in BIT;z:out BIT);    end component    Then   1. What kind of architecture modeling is it ? 2. Compose the portmap statement and the entity. | CO1 | 5 |
| c. | List various object class and write the syntax for declaring object using various object class | CO1 | 5 |
| 3. | a. | Give syntax for the following VHDL statements and with example explain each statement  (1)If statement  (2) case statement | CO1 | 16 |
|  | b. | Distinguish thefollowing in terms of simulation  i)dataflow and behavioral model.  ii) Variable and signal Assignment statement. | CO1 | 4 |
| (OR) | | | | |
| 4. | a. | Develop full adder test bench. | CO1 | 10 |
|  | b. | Design T and RS flip flop. | CO1 | 10 |
| 5. | a. | Construct 4-bit sequential circuit using VHDL that is used to count the number of clock pulses. The up counting and the down counting process in the counter is decided by the control signal. | CO2 | 10 |
|  | b. | With example explain selected signal assignment and conditional signal assignment statement. | CO1 | 10 |
| (OR) | | | | |
| 6. | a. | Design the 4-bit shift register that will accept input data serially and gives output datain parallel. | CO2 | 10 |
|  | b. | A simple module called D implements the following logic equations  Out = (a . b) + c)  The module contains two gate delays 5 ns for and gate 4 ns for OR gate. Write VHDL definition for module D with Delay.\ | CO2 | 5 |
|  | c. | Write the syntax of inertial delay and transport delay | CO1 | 5 |
| 7. | a. | Design Traffic light controller circuit using VHDL. | CO3 | 20 |
| (OR) | | | | |
| 8. | a. | Construct the sequential circuit for the following state diagram. | CO3 | 20 |
|  | | **Compulsory:** |  |  |
| 9 | a. | Show the syntax for function and procedure. | CO1 | 5 |
|  | b. | Develop a package using VHDL for the following function | CO2 | 15 |

ALL THE BEST