Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May– 2017**

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| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | List the various operators and its operation in VHDL. | CO1 | 10 |
| b. | Construct a half adder circuit using VHDL structural modeling. | CO2 | 10 |
| (OR) | | | | |
| 2. | a. | Show and explain a typical design flow process for designing VLSI IC circuits. | CO1 | 10 |
| b. | Design a combinational circuit for the following truth table using VHDL behavioral modeling using IF statement.   |  |  |  |  | | --- | --- | --- | --- | | A | B | C | Y | | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 1 | | 0 | 1 | 0 | 0 | | 0 | 1 | 1 | 1 | | 1 | 0 | 0 | 1 | | 1 | 0 | 1 | 0 | | 1 | 1 | 0 | 1 | | 1 | 1 | 1 | 1 | | CO2 | 10 |
| 3. | a. | Design the following combinational circuit using VHDL Data flow modeling. Each gate has a 5 ns delay and the inverter has a 2 ns delay. | CO3 | 10 |
|  | b. | Discuss various delay models in VHDL. Write the syntax of all delay models. | CO1 | 10 |
| (OR) | | | | |
| 4. | a. | Read the statements and fill the following blanks  TYPE count is RANGE 0 TO 127;  TYPE states IS (idle, decision,read,write);  TYPE word IS ARRAY(15 DOWNTO 0) OF bit;  count'left = \_\_\_\_\_\_\_\_ count'right = \_\_\_\_\_\_\_\_  count'high = \_\_\_\_\_\_\_\_ count'low = \_\_\_\_\_\_\_\_  count'length = \_\_\_\_\_\_\_\_  states'left = \_\_\_\_\_\_\_\_ states'right = \_\_\_\_\_\_\_\_  states'high = \_\_\_\_\_\_\_\_ states'low = \_\_\_\_\_\_\_\_  states'length = \_\_\_\_\_\_\_\_  word'left = \_\_\_\_\_\_\_\_ word'right = \_\_\_\_\_\_\_\_  word'high = \_\_\_\_\_\_\_\_ word'low = \_\_\_\_\_\_\_\_  word'length = \_\_\_\_\_\_\_\_ | CO1 | 15 |
|  | b. | Write syntax of selected signal assignment statement and conditional signal assignment statement. | CO1 | 5 |
| 5. | a. | Develop 8X3 encoder using VHDL. | CO2 | 10 |
|  | b. | With one example explain all the loop statements in VHDL. | CO1 | 10 |
| (OR) | | | | |
| 6. | a. | Design the 4-bit shift register that will accept input data serially and gives output data serially. | CO2 | 10 |
|  | b. | Construct 4X1 multiplexer VHDL test bench. | CO2 | 10 |
| 7. |  | Write ALU VHDL program for the following operation  **ALU**  **ARITHMETIC**  **LOGICAL**  L  M  LSEL  A  B  A SEL  AOUT  LOUT   |  |  |  |  | | --- | --- | --- | --- | | **ASEL** | **AOUT** | **LSEL** | **LOUT** | | ADD | A+B | OR1 | L OR M | | SUB | A-B | AND1 | L AND M | | MUL | A\*B | NAND1 | L NAND M | | DIV | A/B | NOR1 | L NOR M | | AMIX | (A+B)\*(A-B) | EXOR1 | L XOR M | | BMIX | (A\*B)+A | LMIX | (L OR M) AND L | | CO3 | 20 |
| (OR) | | | | |
| 8. |  | Design the following circuit using VHDL.  Image result for moore model state diagram | CO3 | 20 |
|  | | **Compulsory**: |  |  |
| 9 | a. | Compare function and procedure in sub program . | CO1 | 2 |
|  | b. | Develop a VHDL package for fulladder circuit. | CO2 | 15 |
|  | c. | With one example Show how the generics are used in VHDL program. | CO1 | 3 |