Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – April/May – 2017**

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| **Code :** | **14CS2005** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | What are the four main functions of a computer? | CO1 | 4 |
| b. | List and briefly define the main structural components of a computer. | CO1 | 8 |
| c. | What are interrupts? Elaborate the process of interrupt handing. | CO2 | 8 |
| (OR) | | | | |
| 2. | a. | Illustrate with a figure the program flow control with and without interrupts. Indicate the action taken at each stage. | CO2 | 10 |
| b. | What types of transfers must a computer’s interconnection structure (e.g., bus) support? | CO2 | 5 |
| c. | List the features of different types of memory used in a computer system | CO2 | 5 |
| 3. | a. | How does the principle of locality relate to the use of multiple memory levels? | CO2 | 5 |
|  | b. | What is the distinction between spatial locality and temporal locality? | CO1 | 5 |
|  | c. | Elaborate the cache replacement policies with examples. | CO2 | 10 |
| (OR) | | | | |
| 4. | a. | Consider an 8 bit data 11100110 to be stored into memory. Assume that the third data bit is suffering from error and changed from 1 to 0. Compute the hamming code and syndrome word for this data and prove that the third data bit is affected by error. | CO3 | 10 |
| b. | Differentiate static RAM and dynamic RAM. | CO2 | 5 |
| c. | Explain the organization of DRAM | CO2 | 5 |
| 5. | a. | What are the major functions of an I/O module? | CO2 | 5 |
|  | b. | Discuss with suitable diagrams how the DMA mechanism avoids the involvement of processor in any input or output operation. | CO2 | 10 |
|  | c. | Draw the general block diagram of I/O module. | CO1 | 5 |
| (OR) | | | | |
| 6. |  | Explain the two’s complement division algorithm with suitable flowchart. Tracing the algorithm evaluate 5/2. | CO3 | 20 |
| 7. | a. | What are the advantages and disadvantages of using a variable-length instruction format? | CO3 | 5 |
|  | b. | Explain various addressing modes with suitable diagram. | CO2 | 15 |
| (OR) | | | | |
| 8. | a. | Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline? | CO3 | 5 |
|  | b. | Write short notes on control and status registers. | CO2 | 10 |
|  | c. | Compare the performance of a processor with and without instruction pipelining. | CO2 | 5 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Compare and contrast hardwired implementation and a micro programmed implementation of a control unit? | CO2 | 15 |
|  | b. | What is the overall function of a processor’s control unit? | CO2 | 5 |

ALL THE BEST