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**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_\_

**End Semester Examination – Nov/Dec - 2016**

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|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **11MT210/ 12MT211/ MT227** | **Duration :** | **3 hrs** |
| **Sub. Name :** | **Digital Electronics** | **Max. marks :** | **100** |

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| **Q. No.** | **Questions** | | | | **Marks** | | |
| **PART-A(10X1=10 MARKS)** | | | | | | | |
| 1. | Give the symbolic representation of an OR gate. | | | | (1) | | |
| 2. | Simplify A.AB+C.C’D. | | | | (1) | | |
| 3. | Write the truth table of a NOT gate. | | | | (1) | | |
| 4. | Define a Decoder. | | | | (1) | | |
| 5. | What is Odd Parity? | | | | (1) | | |
| 6. | How is a mod-10 counter also called as? | | | | (1) | | |
| 7. | Give the other name for asynchronous circuit. | | | | (1) | | |
| 8. | Define a Multiplexer. | | | | (1) | | |
| 9. | Expand IIL. | | | | (1) | | |
| 10. | How is the electrical energy used by the logic circuit in a specified time called? | | | | (1) | | |
| **PART B(5 X 3= 15 MARKS)** | | | | | | | |
| 11. | | Convert (47)8 to Hexadecimal. | | | | (3) | |
| 12. | | Design a 2x4 Decoder. | | | | (3) | |
| 13. | | What is a register? | | | | (3) | |
| 14. | | Draw the truth table for a D Flipflop. | | | | (3) | |
| 15. | | Explain the operation of CMOS inverter. | | | | (3) | |
| **PART C(5 X 15= 75 MARKS)** | | | | | | |
| 16. | | | . | Simplify the logic expressin  F(a,b,c,d)=∑m(0,3,5,7,8,9,10,12) and draw the simplified circuit. | (15) | |
| (OR) | | | | | | |
| 17. | | |  | Simplify F(A,B,C,D) =∑m(0,2,3,6,7,8,10,12,13) using tabulation method. | (15) | |
| 18. | | |  | Design and implement a Half Adder and Full Adder. | (15) | |
| (OR) | | | | | | |
| 19. | | |  | Design and implement a BCD to Gray Code Convertor. | (15) | |
| 20. | | |  | Briefly explain the following flip flops   1. RS Flip flop b)D Flip flop c)D Flip flop d) T Flip flop | (15) | |
| (OR) | | | | | | |
| 21. | | |  | Design a mod 10 Counter using T flipflop. | (15) | |
| 22. | | |  | Design a synchronous counter to count the sequence 1,2,5,7. Avoid lock condition using T flip flop and draw the state diagram. | (15) | |
| (OR) | | | | | | |
| 23. | | | a. | Design a counter to count numbers from 0 to 6 using T flip flop. | (6) | |
| b. | Explain the operation of a Master- Slave Flipflop. | (9) | |
| 24. | | |  | Explain the properties and Operation of PAL, PLA. | (15) | |
| (OR) | | | | | | |
| 25. | | |  | How are RTL and TTL used to implement a logic circuit. | (15) | |