**Karunya UNIVERSITY**
(Karunya Institute of Technology & Sciences)
(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

Reg.No. _____

# End Semester Examination – Nov/Dec - 2016

**Semester : 2016-17 ODD**
**Code : 10EC205** **Duration : 3 hrs**
**Sub. Name : VLSI DESIGN** **Max. marks : 100**

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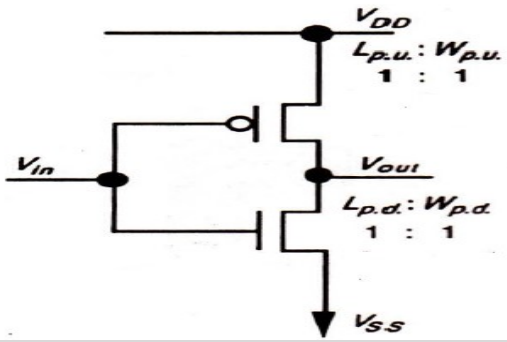
| Q. No. | Questions | Marks |
|---|---|---|
| | **PART-A(10X1=10 MARKS)** | |
| 1. | Define full custom design? | (1) |
| 2. | _____material is used as an insulator in Silicon on Insulator method of fabrication. | (1) |
| 3. | Define Depletion mode transistor? | (1) |
| 4. | Draw the Stick diagram of CMOS? | (1) |
| 5. | Define Sheet Resistance? | (1) |
| 6. | Give the advantages of pseudo NMOS Logic. | (1) |
| 7. | Brief Transport Delay with an example. | (1) |
| 8. | Give the format of component declaration statement. | (1) |
| 9. | State the syntax of CASE statement in VHDL. | (1) |
| 10. | Mention the different types of Modeling in VHDL. | (1) |
| | **PART B(5 X 3= 15 MARKS)** | |
| 11 | Difference between Enhancement and Depletion mode MOSFET | (3) |
| 12 | Draw the stick diagram of 2-input CMOS NAND Gate. | (3) |
| 13 | Find $Z_{p.u}$ : $Z_{p.d}$ ratio and $R_{on}$ of CMOS Inverter(use 5µm MOS Process).   | (3) |
| 14 | Give the difference between signals and variables. | (3) |
| 15 | Write the syntax for entity statement | (3) |
| | **PART C(5 X 15= 75 MARKS)** | |
| 16. a. | Discuss in detail about the different steps of NMOS fabrication process giving a neat schematic. | (15) |
| | (OR) | |
| 17. a. | Explain the different steps of fabrication of SOI (Silicon on Insulator) giving a schematic for every step. | (15) |
| 18. a. | Describe in detail the various regions in CMOS inverter DC characteristics. | |
| | (OR) | |
| 19. a. | Discuss in detail about the λ based design rules for CMOS N-Well Process with neat schematic. | (15) |
| 20. a. | Obtain the expression for area capacitance, and calculate the area capacitance of different layers of MOSFET. | (15) |
| | (OR) | |

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|---|---|---|---|
| 21. | a. | Explain in detail about Dynamic CMOS Logic with necessary diagrams and draw the Dynamic CMOS Logic for the function $Z = A(B+C) + \overline{DE}$ | (10) |
| | b. | Obtain the 3 Input NAND gate using Clocked CMOS Logic. | (5) |
| 22. | a. | Design a T Flip-flop in Behavioral modeling using VHDL. | (5) |
| | b. | Give the different data types and explain about scalar data type. | (10) |
| | | (OR) | |
| 23. | a. | Write a Program for 2 bit magnitude comparator using structural modeling in VHDL. | (15) |
| 24. | a. | Describe in detail about concurrent signal assignment statement and selected signal assignment statement with an example. | (10) |
| | b. | Design a 3 : 8 Decoder using VHDL in Data flow modeling. | (5) |
| | | (OR) | |
| 25. | a. | Give the significance of Test Bench and Write a test bench program using VHDL Code for Full Adder. | (10) |
| | b. | Write short notes on Wait statement. | (5) |

ALL THE BEST