**Karunya University**

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examinations – June 2016**

**Subject Title: VHDL Time : 3 hours**

**Subject Code: 14EC2068 Maximum Marks: 100**

**Answer ALL questions (5 x 20 = 100 Marks)**

1. a. With examples explain in detail about different scalar data types. (15)

b. Explain the steps in IC design process. (5)

**(OR)**

2. a. List the types of data operators available in VHDL with examples. (8)

b. Explain in detail about data objects with examples. (12)

3. a. Write the entity description for AND-OR-INVERT circuit and also explain about architecture body. (14)

b. Write VHDL code for the full adder by using data flow modeling. (6)

**(OR)**

4. a. Explain in detail about conditional signal assignment statement in VHDL with an example. (15)

b. By using CASE statementwrite VHDL code for a 4X1 multiplexer. (5)

5. a. Explain in detail about selected signal assignment statement in VHDL with an example. (12)

b. Write structural modeling for half adder using VHDL. (8)

**(OR)**

6. a. Give the difference between variable and signal assignment statement. (8)

b. Write a VHDL Program for four bit full adder, using the structural description .Draw its basic structure showing the inputs and outputs signals. (12)

7. a. Explain in detail about test bench and write the test bench for full adder. (15)

b. Write short notes on procedure. (5)

**(OR)**

8. a. Design a 2 bit magnitude comparator in Behavioral modeling using VHDL (use **if-then- else** OR **CASE statement**). (10)

b. Write short notes on component declaration statement. (5)

9. **Compulsory:**

a. Explain in detail about Traffic light Controller functions. (16)

b. Write in detail about delta delay. (4)