**Karunya University**

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examinations – June 2016**

**Subject Title: DIGITAL ELECTRONICS Time : 3 hours**

**Subject Code: 14EC2001 Maximum Marks: 100**

**Answer ALL questions (5 x 20 = 100 Marks)**

1. a. Place the equation J = f (A,B,C,D) = (A + B' +C) (A' + D) into the proper canonical form. Convert the obtained canonical form into SoP form and draw the logic diagram.

(14)

b. With examples explain about different types of non-weighted codes. (6)

**(OR)**

2. a. Perform the following conversion (15)

i. 235 decimal to hexadecimal ii. 237 octal to decimal

iii. 444.456 decimal to octal iv. 2D5 hex to binary

v. 2F3 hex to decimal

b. Use Karnaugh map to simplify the following Boolean expression.

Y = Σ(1, 2, 4, 6, 7) (5)

3. a. Design a 2 bit Magnitude Comparator Circuit. (16)

b. Draw the block diagram of 4bit binary parallel adder circuit. (4)

**(OR)**

4. a. Design a BCD to Excess3 code converter circuit. (10)

b. Design a 1 to 4 Demultiplexer circuit. (10)

5. Design a 3 bit binary up/down counter using JK flipflop.

**(OR)**

6. a. Design a modulo-5 synchronous counter using T flip-flop. (14)

b. Explain the excitation table for SR and D flipflops. (6)

7. With respect to clock pulses, explain the operations of

a. 4 bit SISO shift register (10)

b. 4 bit SIPO shift register (10)

**(OR)**

8. Mention the difference between synchronous and asynchronous counters and explain the operation of Johnson counter with respect to the clock pulse.

**Compulsory:**

9. Find minimum SoP for the following PoS and implement using (2)

F(A,B,C,D)= π(3,4,6,7,11,12,13,14,15)

a. PROM (5)

b. PLA (5)

c. Describe the operation of a CMOS inverter with a neat diagram. (8)