**Reg. No. \_\_\_\_\_\_\_\_**

**Karunya University**

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination - June 2011**

**Subject Title: DIGITAL SIGNAL PROCESSING Time: 3 hours**

**Subject Code: EI262 Maximum Marks: 100**

#### **Answer ALL questions**

**PART – A (10 x 1 = 10 MARKS)**

1. What are the main advantages of FFT?

2. Compute the N-point DFT of x(n) = δ(n).

3. State Shannon's Sampling theorem.

4. Mention two properties of FIR filter.

5. Give two transformations to digitize an analog filter.

6. What is called pre warping?

7. List some applications of P-DSPs.

8. What is the circular addressing mode of DSP processor.

9. What is the use of instruction RET in TMS processor?

10. List the onchip peripherals in ‘C5x.

**PART – B (5 x 3 = 15 MARKS)**

11. List the various applications of a DSP processor.

12. Draw the basic butterfly diagram for DIT algorithm.

13. What are the elements present in central processing unit.

14. Write the equation of Blackman window.

15. What is meant by memory mapped register?

**PART – C (5 x 15 = 75 MARKS)**

16. Find the DFT of the sequence x(n) = {1, 2, 3, 4, 4, 3, 2, 1}using Decimation-in-Time FFT.

(OR)

17. Find the DFT of the sequence x(n) = {0.5, 0.5, 0.5, 0.5, 0, 0, 0, 0} using Decimation-in-Frequency FFT.

18. Design a low pass filter using rectangular window with passband gain of unity, cut off frequency of 1000Hz and working at a sampling frequency of 5 kHz. The length of the impulse response should be 7.

(OR)

19. What are the steps involved in designing an FIR filter using Frequency Sampling method?

20. Obtain the cascade and parallel realization of the system described by

y(n)= -0.1y(n-1)+0.2y(n-2)+3x(n)+3.6x(n-1)+0.6x(n-2).

(OR)

21. Explain in detail about IIR filter design by the bilinear transformation.

22. Describe the multiplier and accumulator unit in DSP processor.

(OR)

23. Discuss in detail the different types of addressing modes in DSP processor.

24. Explain the architecture ofTMS320C5X DSP processor.

(OR)

25. Write a program to perform addition of two 64 bit numbers.