**Reg. No. \_\_\_\_\_\_\_\_**

**Karunya University**

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination - June 2011**

**Subject Title: TESTING AND TESTABILITY OF ELECTRONICS SYSTEMS**

**Time: 3 hours**

**Subject Code: 10EC313 Maximum Marks: 100**

**Answer ALL questions (5 x 20 = 100 Marks)**

1. **Compulsory**:

Discuss about the Path sensitization and D algorithm.

2. a. Discuss about the logical fault models. (10)

b. Explain about Fault equivalence and Fault Location in Combination circuits. (10)

(OR)

3. Explain about the fault detection and redundancy in sequential circuit.

4. Write short notes on:

a. Serial fault simulation (10)

b. Parallel fault simulation (10)

(OR)

5. a. Discuss about the concurrent fault simulation technique. (10)

b. Explain the Three valued Deductive Fault Simulation. (10)

6. a. Explain about board level and system level DFT approach. (10)

b. Briefly explain about Ad- Hoc design for Testability Techniques. (10)

(OR)

7. The following question deals with IEEE 49.1

a. Discuss various application for the capability to load the instruction Register with system status information. (10)

b. Discuss how the on-chip test bus circuitry can be tested. (10)

8. a. Explain about LSSD On – Chip Self – Test (LOCST). (10)

b. Discuss about concurrent BIST Architecture. (10)

(OR)

9. a. Explain a Centralized and Separate Board – level BIST Architectures. (10)

b. Discuss about the Pseudorandom Testing. (10)