Credits 4:0:0

Course Objective
To study the concepts on different levels of power estimation and optimization techniques.

Outcome
To design chips used for battery-powered systems and high-performance circuits not exceeding power limits.

Unit I
Simulation Power Analysis: Need For Low Power VLSI Chips- Charging And Discharging Capacitance- Short Circuit Current- Leakage Current- Static Current- Basic Principles of Low Power Design- Gate Level Logic Simulation- Architectural Level Analysis

Unit II
Circuit and logic level power Estimation: Transistor and Gate Sizing- Equivalent Pin Ordering- Network Reconstructing and Reorganization- Gate Reorganization- Signal Gating- Logic Encoding- State Machine Encoding- Pre-Computation Logic- Power Reduction in Clock Networks- CMOS Floating Node- Low Power Bus- Delay Balancing

Unit III

UNIT IV
Circuit Design techniques and SRAM Architecture

Unit V

Text Books
Reference Books